6. Video, Audio and Sub-picture Decoding

Figure 35 shows a simplified block diagram of the operation of the **ZR36710**. This section explains the front-end of the diagram regarding bitstream selection, decryption, stream demultiplexing, and decoding. This section does not go into detail on how the **ZR36710** handles bitstreams provided at a constant rate via the CD-DSP interface and this information is provided in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams” and in microcode release notes. Section 14. “Annex C: Programming Sequence for Playback” complements this section by giving a step-by-step sequence of instructions on how to perform playback of the various types of bitstreams supported.

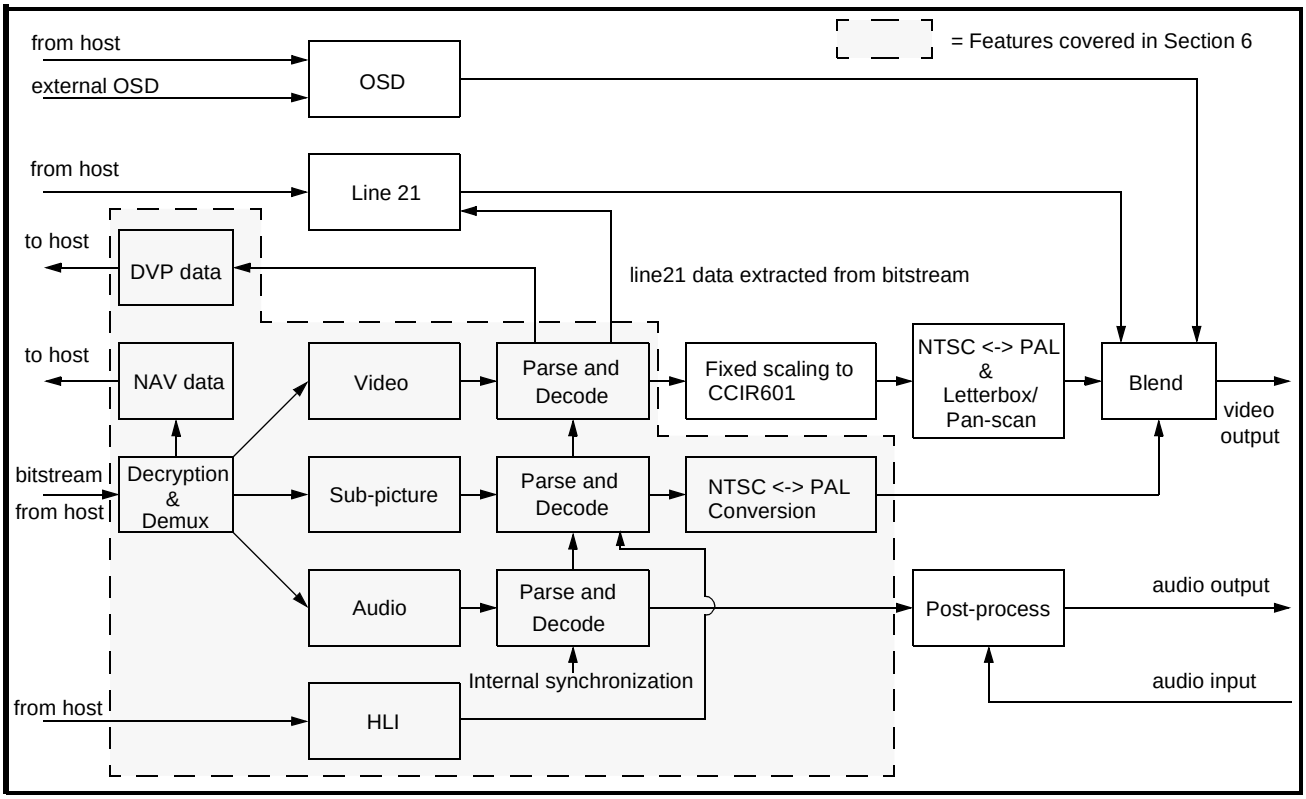

FIGURE 35. Simplified block diagram of **ZR36710** with focus on decoding

6.1 Bitstream Sources

Bitstream data is provided to the **ZR36710** via the host bus, DVD-DSP or CD-DSP interface. The host must configure the device to accept this data from one of these three interfaces as explained in Section 4. “Hardware Interfaces” via the *SysConfig* and *SDConfig*[1] set-up parameters as shown in Table 57 .

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

TABLE 57. Configuring the bitstream source port: DVD-DSP, CD-DSP or host bus interface

***SysConfig* (0x00)**						
15, 14	**13**	**12**	**11 - 4**	**3**	**2**	**1, 0**
reserved	NumDRAMDev	CodeSource	CodBurstLen	DecBypass	HACKMode	reserved

Reserved bits must be 0.	
CodeSource	0 = DVD-DSP/CD-DSP interface provides bitstream data. 1 = Host bus interface provides bitstream data.
CodBurstLen	If CodeSource = 0, allowed values are 16, 32, 64. If CodeSource = 1, allowed values are 4, 8, 16, 32, 64.

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	0	CDPeriod	0	REQPol	VALIDPol	SOSPol	STRBPol	0	CDBitSwap	0

DVDREQSync	0 = DVDREQ is not synchronous with DVDSTRB. Must be 0 if not applicable. 1 = DVDREQ is synchronous with DVDSTRB.
IFMode	0 = DVD-DSP interface used. Must be 0 if host bus interface is used to transfer bitstream. 1 = CD-DSP interface used. ***HWID*** = GND.
CDEdge	0 = CD-DSP interface signals are sampled on falling edge of CDCLK. Must be 0 if not applicable. 1 = CD-DSP interface signals are sampled on rising edge of CDCLK.
CDJust	00b = CDDAT data is left-justified. Must be 00b if not applicable. 01b = CDDAT data is left-justified with one CDCLK cycle delay. 10b = CDDAT data is right-justified.
CDPeriod	00b = CDFRM period is 32 CDCLK cycles. Must be 00b if not applicable. 01b = CDFRM period is 48 CDCLK cycles. 10b = CDFRM period is 64 CDCLK cycles.
REQPol	0 = DVDREQ is active-low. Must be 0 if not applicable. 1 = DVDREQ is active-high.
VALIDPol	0 = DVDVALID is active-low. Must be 0 if not applicable. 1 = DVDVALID is active-high.
SOSPol	0 = DVDSOS is active-low. Must be 0 if not applicable. 1 = DVDSOS is active-high.
STRBPol	0 = DVD-DSP signals are sampled on falling edge of DVDSTRB. Must be 0 if not applicable. 1 = DVD-DSP signals are sampled on rising edge of DVDSTRB.
CDBitSwap	0 = No bit swapping on CD-DSP interface. Must be 0 if not applicable. 1 = Bit swapping (reverse order l.s. to m.s.) per word on CD-DSP.

The type of disc supported (if data is received through the DVD-DSP or CD-DSP interfaces) and/or the type of bitstream parsed and decoded is selected through the *DiscType*[1] and *BitstreamSelect*[1] set-up parameters.

TABLE 58. Selecting the Bitstream Type to Parse and/or Decode via *DiscType* and *BitstreamSelect*

***DiscType* (0x38)**		
15 - 2	**1**	**0**
reserved	SOSDelay	MajorType
Reserved bits must be 0.		
MajorType	0 = DVD disc. Must be 0 if CodeSource = 1. 1 = CD disc.	

***BitstreamSelect* (0x40)**		
15 - 11	**10 - 1**	**0**
CBSelect	reserved	VidEntry
Reserved bits must be 0.		
CBSelect	00000b = VideoCD and CD-I (FMV) sectors with embedded MPEG-1 system-multiplexed bitstream. 00010b = DVD video object (VOB) sectors. 00100b = CD-DA PCM stereo audio sectors. 00101b = VideoCD auxiliary sectors via DVD-DSP/CD-DSP interface to be stored in SDRAM after Mode 2 Form 1 sector block decoding. 00110b = DVD navigation file sectors (e.g. VTSI, VMGI) via DVD-DSP interface to be stored in SDRAM. 00111b = MPEG-1 system (ISO 11172-1,2,3) or MPEG-2 program (ISO 13818-1,2,3) stream. 01100b = MPEG-1 video (ISO 11172-2) or MPEG-2 video (ISO 13818-2) elementary stream. 01101b = MPEG-1 video (ISO 11172-2) or MPEG-1 audio (ISO 11172-3) elementary stream packetized (PES) according to ISO 11172-1. Also supported is MPEG-1 video (ISO 11172-2), MPEG-1 audio (ISO 11172-3), MPEG-2 video (ISO 13818-2) or MPEG-2 audio (ISO 13818-3) elementary stream packetized (PES) according to ISO 13818-1. Also supported is AC-3 audio, PCM audio, or sub-picture elementary stream packetized (PES) according to the DVD Specification 1.0. 01111b = MPEG-1 audio (ISO 11172-3) or MPEG-2 audio (ISO 13818-2) elementary stream. 10110b = AC-3 audio elementary stream. 11000b = LPCM audio elementary stream according to the DVD Specification 1.0. All other combinations are reserved and must not be used.	

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

The DVD-DSP, CD-DSP and host bus interfaces support the following combinations of *CBSelect* as described in Table 58 above.

- DVD-DSP interface: *CBSelect* = 00000b, 00010b, 00100b, 00101b, 00110b.
- CD-DSP interface: *CBSelect* = 00000b, 00100b, 00101b.
- Host bus interface: *CBSelect* = all supported combinations.

For bitstreams transferred via the DVD-DSP or CD-DSP interface, they must be of the formats described in Table 59 below.

TABLE 59. DVD and CD formats via DVD-DSP and CD-DSP interfaces

Data Type	Interface	Format
DVD	DVD-DSP	Any sector (2048 - 2064[a] bytes)
VideoCD	DVD-DSP or CD-DSP	Mode 2 Form 1 (2352 bytes) Mode 2 Form 2 (2352 bytes) CD-DA (2352 bytes)
CD-I (FMV)	DVD-DSP or CD-DSP	Mode 2 Form 2 (2352 bytes) CD-DA (2352 bytes)
CD-DA	DVD-DSP or CD-DSP	CD-DA (2352 bytes)

a. Programmable to 2048 (sector data), 2054 (sector data + CPR_MAI) or 2064 (sector data + 12 bytes header + 4 bytes trailer).

DVD Sector Processing

The DVD sector length is 2064 bytes of which 2048 bytes are data. The sector size that the device will accept via the DVD-DSP interface is programmable between 2048 to 2064 bytes. The sector size is selected by the *SOSDelay* bit of the *DiscType* set-up parameter as shown in Table 60 .

TABLE 60. Selecting the DVD Sector Size for the DVD-DSP Interface

***DiscType* (0x38)**			
15 - 2		**1**	**0**
reserved		SOSDelay	MajorType
Reserved bits must be 0.			
SOSDelay	0 = DVD-DSP device does not transmit the ID and IED bytes (first 6 bytes) of each DVD sector. Must be 0 if MajorType = 1 or if DVD-DSP interface is not used. 1 = DVD-DSP transmits ID and IED bytes of each DVD sector.		

The *SOSDelay* bit will indicate to the DVD-DSP interface whether or not to expect the ID and IED bytes of the sector (the first 6 bytes), but the DVD-DSP interface still needs to know whether or not to expect the CPR_MAI bytes (the next 6 bytes) immediately prior to the 2048 data bytes. This information on how to inform the **ZR36710** that the DVD-DSP device provides the CPR_MAI bytes is contained in a separate application note as explained in Section 6.2 “DVD Authentication and Decryption”.

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Phone (408) 919-4111 Fax (408) 919-4122

CD Sector Processing

The following lists which sectors are and are not supported:

- Mode 0: Discarded by the **ZR36710**.
- Mode 1 (CD-ROM): Supported.
- Mode 2 Form 1 (VideoCD): Supported.
- Mode 2 Form 2 (CD-I (FMV) and VideoCD): Supported.
- DA (CD-I (FMV), VideoCD and CD-DA): Supported.

6.2 DVD Authentication and Decryption

The **ZR36710** supports DVD decryption through both its DVD-DSP and host bus interfaces (the CD-DSP interface is excluded). In addition, both interfaces support DVD-ROM drive authentication for **ZR36710** applications in a PC environment. This section gives an overview of the authentication and decryption process of the **ZR36710**. The details of the **ZR36710** authentication protocol with the host, enabling of the decryption circuit and key transfer protocol (e.g. set-up parameter settings) can only be revealed to CSS (Content Scramble System) licensees. This confidential information is provided in a separate application note and is required to implement the **ZR36710** in both DVD player and DVD-PC applications. To obtain this application note, please contact Zoran's Customer Support and have available proof of a CSS license. For more information on how to obtain a CSS license, please contact Zoran's **ZR36710** Marketing Department.

6.2.1 Decryption Overview

Each encrypted DVD disc contains two types of "keys" that are used by the **ZR36710** in the decryption process. These keys, described in Table 61 , are required by the decryption circuit of the device in order to properly descramble the data prior to decoding.

TABLE 61. Decryption - Disc and Title Key Description

Key	Description
Disc	Many DVD discs contain encrypted titles. If one or more titles on a disc are encrypted, then the disc itself is considered encrypted. Each encrypted disc has one "disc key" that is used in conjunction with the title keys (explained below) to decrypt each title on the disc.
Title	On an encrypted DVD disc, some of the titles (e.g. *.VOB files) are encrypted. The navigation files (e.g. *.IFO, *.BUP files) are not encrypted. Each encrypted title has a "title key" that is used with the disc key that enables decryption of that title.

Key Transfer to the ZR36710 and Decryption

In order to decrypt the encrypted sectors of a title, first the disc key and then the title key are transferred to the **ZR36710** before transferring the bitstream of the encrypted title. These keys are used by the decryption hardware to properly decrypt the encrypted sectors. Non-encrypted sectors are simply passed through the decryption circuitry to the decoding circuitry of the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.2.2 Authentication Overview

In a PC environment, authentication between the DVD-ROM drive and the **ZR36710** is used to guarantee that encrypted data transfer can take place. Without proper authentication, no data will be transferred from an encrypted DVD into the PC's memory. This prevents copying of DVD files from the disc onto a computer's hard drive or other storage device.

The first step of the authentication process requires the **ZR36710** to query the DVD-ROM drive and verify that it is an "authorized" encrypted data source. If the drive's response is not what the device expected, then the authentication fails.

If the first step of this process succeeds, then the second step of the authentication process requires the DVD-ROM drive to query the **ZR36710** and verify that is an authorized decoder. If the device's response is not what the DVD-ROM drive expected, then the authentication fails. If the authentication passes, then the DVD-ROM drive may pass the keys and encrypted data to the **ZR36710**.

6.2.3 Decryption Bypass Mode

Without a CSS license, the **ZR36710** may still be used to decode unencrypted content. In this case, it is necessary to configure the device for "bypass" mode in which the decryption circuitry is disabled. This is done by correctly setting the *DecBypass* bit of the *SysConfig*[1] parameter to 0. If the DVD-DSP interface is used for bitstream transfer, the *DVDReqEnable* bit of the *PlaybackMode*[1] parameter must be cleared. Table 62 shows these two parameters required to configure the device for decryption bypass mode.

TABLE 62. Decryption Bypass Mode Parameter Settings

***SysConfig* (0x00)**						
15, 14	**13**	**12**	**11 - 4**	**3**	**2**	**1, 0**
reserved	NumDRAMDev	CodeSource	CodBurstLen	DecBypass	HACKMode	reserved
Reserved bits must be 0.						
DecBypass	0 = Internal decryption circuit is disabled (bypass). 1 = Internal decryption circuit is enabled.					

***PlaybackMode* (0x41)**							
15 - 10	**9**	**8, 7**	**6**	**5**	**4**	**3**	**2 - 0**
reserved	LastPic	reserved	VidFloat	reserved	Black	DVDReqEnable	reserved
Reserved bits must be 0.							
DVDReqEnable	0 = DVDREQ is enabled. This is normal operation. 1 = DVDREQ is disabled. This is a special operation mode for title key transfer during decryption as explained in a separate application note.						

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.3 Audio, Video and Sub-picture Stream ID Selection

Before the **ZR36710** begins bitstream acquisition, decryption, demultiplexing, parsing and decoding, the host must identify (if necessary, depending on the type of bitstream to decode) which audio, video and sub-picture streams to decode. This selection is done via *AudSID*[1], *VidSID*[1] and *SPSID*[1].

TABLE 63. Audio, Video and Sub-picture stream ID selection

Set-up Parameter	Value	Function
AudSID (Audio) Only combinations specified can be used. No other combinations are allowed.	0x0000	First MPEG audio stream ID encountered. (Only for *CBSelect* = 00000b, 00010b or 00111b)
	0x0008	First AC-3 audio sub-stream ID encountered in a private1 stream. (Only for *CBSelect* = 00010b)
	0x000A	First PCM audio sub-stream ID encountered in a private1 stream. (Only for *CBSelect* = 00010b)
	0x0080 - 0x0087	AC-3 audio sub-stream ID in a private1 stream to decode. (Only for *CBSelect* = 00010b)
	0x00A0 - 0x00A7	PCM audio sub-stream ID in a private1 stream to decode. (Only for *CBSelect* = 00010b)
	0x00C0 - 0x00DF	MPEG audio stream ID to decode. (Only for *CBSelect* = 00000b, 00010b or 00111b)
	0x00BD	Audio port passes through private1 stream data without processing. (Only for *CBSelect* = 00000b or 00111b)
	0x00BF (1st case)	Audio port passes through private2 stream data without processing. (Only for *CBSelect* = 00000b or 00111b)
	0x00BF (2nd case)	Audio data is output. (Only for *CBSelect* = 00100b, 01101b, 01111b, 10110b or 11000b)
	0x00FF	Audio stream is discarded. No audio data is decoded nor output.
VidSID (Video) Only combinations specified can be used. No other combinations are allowed.	0x0000	First video stream ID encountered. (Only for *CBSelect* = 00000b, 00010b or 00111b)
	0x00E0 - 0x00EF (1st case)	Video stream ID to decode. (Only for *CBSelect* = 00000b, 00010b or 00111b)
	0x00EF (2nd case)	Video stream is decoded and output. (Only for *CBSelect* = 01100b or 01101b)
	0x00FF	Video stream is discarded. No video data is decoded.
SPSID (sub-picture) Only combinations specified can be used. No other combinations are allowed.	0x0000	First sub-picture sub-stream ID encountered in a private1 stream. (Only for *CBSelect* = 00010b)
	0x0020 - 0x003F	Sub-picture sub-stream ID in private1 stream to decode. (Only for *CBSelect* = 00010b)
	0x00FF	Sub-picture stream is discarded. Must be set to 0x00FF if *CBSelect* does not equal 00010b.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

As indicated in Table 63 if the particular stream ID to decode is not known, the **ZR36710** will decode the stream with the first ID encountered if the stream ID is set to 0x0000. Stream IDs can be changed during playback (in between a **start**[1] command and either the end of the bitstream or an **end_playback**[1] command), however, for changing of audio stream IDs, please refer to Section 14.5 "Also For: Changing Audio Parameters During Playback".

6.4 Begin Playback Process - "start" Host Command

The term "playback" is defined as bitstream acquisition, decryption, demultiplexing and decoding. The playback process begins when the host issues a **start** command and **ZR36710** receives bitstream. At this time, the **ZR36710** begins to request data via either the DVD-DSP or host bus interfaces. If the CD-DSP interface is used, the **ZR36710** begins to accept and process data provided on the CD-DSP interface at this time. Section 6.11 "Host Commands and Control over the Playback Operation" explains the available host commands in further detail.

6.5 Stream Demultiplexing

The DVP is responsible for demultiplexing the bitstream. To properly demultiplex the bitstream, the DVP must have the following:

- Correct DVP microcode loaded to the **ZR36710** associated with the incoming bitstream.
- Correct setting for *CBSelect*[2] that matches the incoming bitstream.
- Correct stream IDs.

Separating Video, Audio, Sub-picture and NV_PCK Data into SDRAM

The DVP will retrieve data from the coded data FIFO that is filled by either the DVD-DSP, CD-DSP or host bus interfaces. This data is then parsed by the DVP, copying packets of video, audio and sub-picture (if applicable) of the appropriate stream ID to buffers in SDRAM. Packets with other stream IDs are discarded. The DVP strips the pack/packet header information from each of these three streams and copies the elementary stream data to the SDRAM buffers.

If the DVP is parsing a DVD VOB stream (*CBSelect* = 00010b), the NV_PCKs at the beginning of each VOBU (refer to DVD Specifications 1.0 for explanations on VOB and VOBU) are zero-padded and copied into a buffer in SDRAM. Once copied into this NAV buffer, the host may retrieve this data via the protocol explained in Section 5.10 "Reading the NAV Buffer in SDRAM - Reg. 0xA". In order to support sub-picture hilighting (HLI), the host must retrieve the HLI portion of the NV_PCK and write part of this data to the appropriate set-up parameters associated with HLI support as explained in Section 6.8 "Sub-Picture Decoding with HLI Support".

1. See Section 6.11 "Host Commands and Control over the Playback Operation" for an explanation on writing host commands to the **ZR36710**.
2. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

Buffer Fullness Indication

The fullness of each of these buffers can be checked by the host through the Sub-Picture, Video and Audio Code Buffer Status Registers[1]. The buffer sizes for each type of data meet the requirements of worst-case DVD bitstreams. As long as the encoding process done for each bitstream adhered to the buffering requirements for that particular type of bitstream (DVD, VideoCD, etc.) then each of these buffers will not become empty as long as the system provides the multiplexed bitstream at the minimum required rate for that bitstream.

Should a particular buffer become full or empty (e.g. encoding of the bitstream ignored the buffering requirements), the **CODBUFIRQ** bit in the ISR[2] is set to 1. If the corresponding bit in the IMR is cleared, an interrupt is generated to the host. To see which particular buffer became full/empty, the host can check the **VCBE**, **VCBF**, **ACBE**, **ACBF** and **SPCBF** bits of the **STATUS0**[3] register.

6.6 Video Decoding

The term “video decoding” as explained in this section refers to the following steps handled by the **ZR36710**:

- The **ZR36710** retrieves the video stream data from the video code buffer in the SDRAM.
- The stream is decoded, extracting relevant sequence header, GOP header, picture header, sector addresses (VideoCD) and user data information and buffering it in a FIFO for optional host retrieval.
- The reconstructed pictures are presented to a video processing unit (VPU) in their presentation order taking into consideration the need to repeat or drop fields/frames due to A/V synchronization or frame rate conversion.

The VPU will do the necessary processing on the decoded image to support panning (e.g. Pan-scan support), fixed scaling to CCIR-sized interlaced fields, pixel aspect ratio conversion for NTSC <-> PAL conversion, display aspect ratio conversion (e.g. Letterbox and Pan-scan support) and placement of the video in the image area. These features are explained in Section 7. “Video Scaling and Panning”. The output of the VPU is passed on to a blending circuit which adds the sub-picture with HLI (for DVD .VOB streams only) and OSD information onto the video data that is output on the pixel bus as explained in Section 10. “Video Blending”.

To properly decode the video data, the **ZR36710** must have the following:

- Correct DVP microcode[4] loaded to the **ZR36710** associated with the incoming bitstream.
- Correct setting for *CBSelect*[4] that matches the incoming bitstream.

1. See Section 5.12 “Code Buffer Status Registers - Reg. 0xC, 0xD, 0xE (Read)” for an explanation on reading the code buffer status registers.
2. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.
3. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.
4. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters and microcode to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.6.1 Extracting Useful Video Data for Optional Host Retrieval

The DVP parses the video data for relevant information to be used in the decoding process. Some of this information is provided to the host. The **PICTYPE** bits of the **STATUS1**[1] register indicate the type of picture currently being decoded by the **ZR36710**:

- **PICTYPE** = 00b, No MPEG picture is currently being decoded.
- **PICTYPE** = 01b, I-picture is currently being decoded.
- **PICTYPE** = 10b, P-picture is currently being decoded.
- **PICTYPE** = 11b, B-picture is currently being decoded.

The **FRAME/FIELD#** bit of the **STATUS1**[1] register indicates whether the type of picture being decoded is a field-picture or a frame-picture:

- **FRAME/FIELD#** = 0, Picture being decoded is an MPEG-2 field picture.
- **FRAME/FIELD#** = 1, Picture being decoded is an MPEG-1 or MPEG-2 frame picture.

The DVP also provides data to the host through the 64-word DVP output FIFO (DVPO_FIFO). The type of data copied into this FIFO is a combination of the following:

- VideoCD user data or DVD GOP header user data.
- Sequence header and sequence extension header information.
- Picture header and picture extension header information.
- VideoCD sector address.

Once all relevant types of data are completely copied to the DVPO_FIFO, the **DVPOBF** bit in the ISR[2] is set to 1. If the corresponding bit in the IMR is cleared, an interrupt is generated to the host. The data is retrieved via the DVP Data Register as explained further in Section 5.6.2 “Reading Data from the DVP Data Register”.

6.6.2 Frame Rate Conversion

Standards conversion of the decoded images pertains to three attributes: Frame rate, display frame aspect ratio and pixel aspect ratio. Display frame aspect ratio and pixel aspect ratio conversion is explained in Section 7. “Video Scaling and Panning”. This section explains the frame rate conversion process of the **ZR36710**.

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.
2. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.

The **ZR36710** supports two video display frame rates as specified by the *VidFPS*[1] set-up parameter:

- 29.97 (30/1.001 to be exact - NTSC) fps.
- 25 (PAL) fps (frames per second).

The following coded picture rates (MPEG-1) and frame rates (MPEG-2) as specified by the picture rate (MPEG-1) or frame rate (MPEG-2) values found in the sequence header are supported:

- 23.976 pps (pictures per second - MPEG-1) or fps (frames per second - MPEG-2).
- 25 pps (MPEG-1) or fps (MPEG-2).
- 29.97 pps (MPEG-1) or fps (MPEG-2).

If the picture (MPEG-1) or frame (MPEG-2) rate of the coded video does not match the display frame rate of the video output, automatic frame rate conversion is performed. Frames/fields are also discarded/ repeated for A/V sync purposes as explained in Section 6.10 “A/V Synchronization”.

6.7 Audio Decoding and Audio Post-Processing

Audio decoding is performed by the ADP of the **ZR36710**. The ADP retrieves the audio data from the audio code buffer in SDRAM, decodes the data, and presents the audio data in PCM format on the audio port. Audio data may be presented in S/PDIF format (either coded data or PCM) on the S/PDIF connector of the audio port.

The ADP contains the ability to decode/output various types of data (e.g. MPEG-1 (Layer II), AC-3 and PCM). Many functions that pertain to the ADP decoding capabilities are built into its ROM. Other functions are provided via downloadable ADP microcode[2]. The ADP microcode release notes will indicate which functions require the additional microcode and which can be accessed within the ROM.

Audio frames are dropped or paused as required to maintain A/V sync when the ADP is operating in “clock master” mode. In “audio master” mode, the ADP will adjust **SCLK** as necessary to maintain that the audio clock is the master in which the video and sub-picture decoding may lock to. Details of A/V sync are explained in Section 6.10 “A/V Synchronization”. The audio stream ID (*AudSID*[1] set-up parameter) may be changed during decoding as detailed in Section 14.5 “Also For: Changing Audio Parameters During Playback”.

Audio post-processing is explained in a separate application note available by request from Zoran.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 12.5 “Microcode Loading and Debug Commands” for an explanation on loading ADP microcode.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.8 Sub-Picture Decoding with HLI Support

The **ZR36710** parses out the sub-picture data from a DVD bitstream (*CBSelect*[1] = 00010b) and copies it to the sub-picture code buffer within the SDRAM. The SPUs are stored in the buffer in the order of their appearance in the bitstream, which is also the order of their display.

Prior to sub-picture decoding, the sub-picture palette must be loaded into the *SPPalette*[1] set-up parameter. This palette is the PGC_SP_PLT portion of the PGCI data retrieved by the host from the navigation files of a DVD. Refer to the DVD Specifications 1.0 for further details regarding PGC_SP_PLT and PGCI data.

While demultiplexing the DVD bitstream, the **ZR36710** will extract the NV_PCKs and provide it to the host as explained in Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”. This NV_PCK information contains the sub-picture highlighting (HLI) information for the sub-picture(s) within the VOBU identified by the extracted NV_PCK. Refer to the DVD Specifications 1.0 for further details regarding NV_PCK, HLI and VOBU information. The HLI information retrieved from the device is re-entered into HLI-related set-up parameters which instruct the **ZR36710** to properly execute the highlighting of sub-pictures.

Sub-pictures are automatically decoded, converted to the proper color, blended with the video and displayed at the proper time and position on the display by the **ZR36710**. The host only has to indicate which DCSQs (as explained in the DVD Specifications 1.0) trigger display of SPUs via the *SPSwitch*[1] set-up parameter.

Automatic vertical scaling of the sub-picture display for NTSC <-> PAL conversion is indicated through the *SPScale*[1] set-up parameter. The sub-pictures are scaled, but not their position on the display.

6.8.1 Valid Period of Sub-Picture

The valid period of an SPU is from its PTS (the PTS in the packet header of the first packet of the SPU) until the PTS of the next SPU. In cases of still picture display, the SPU is valid until the still picture is terminated by the host (even if the still termination is before the PTS of the next SPU). An SPU is displayed only within its valid period, and only if it is enabled by the host, and turned on by one of the start display (DCSQ) commands.

According to the DVD specs, the PTS’s of the SPU’s are aligned with video top field timing (the explicit or implicit PTS of the top field output from the video decoder).

6.8.2 Host Control over the Sub-Picture Function

The DVD bitstream supports up to 32 interleaved sub-picture streams, denoted 0 to 31. They are distinguished by their sub_stream_id DVD parameter, which appears in the sub-picture packet header. Typically, there are different streams for different languages, and in each language different streams for different aspect ratio correction methods (Wide, Pan-scan, Letterbox).

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

The *SPSID*[1] set-up parameter defines which stream should be decoded by the **ZR36710**. Valid values for this parameter are tabulated in Section 6.3 “Audio, Video and Sub-picture Stream ID Selection”. Only SPUs of this stream will be stored and decoded. When a new stream number is written by the host, the **ZR36710** changes the sub-picture stream, and starts decoding the new stream.

Definition of Active Area For Proper Sub-Picture Placement

For the **ZR36710** to properly position the sub-picture, an active video area of 720x480 for NTSC or 720x576 for PAL must be specified by the *ActiveStartX*, *ActiveStartY*, *ActiveEndX*, *ActiveEndY*, *ActiveSizeX* and *ActiveSizeY*[1] set-up parameters as explained in Section 4.5.4 “Definition of the Active Area, Image Area and Background Color”.

Enable/Disable Sub-Picture Display

There are two levels of enabling sub-picture display, determined by bits (1,0) of the *SPSwitch*[1] set-up parameter as shown in Table 64 . Note that only the actual display of the sub-picture data is affected. Decoding continues according to the timing information in the bitstream and the value of the **SCLK** counter.

TABLE 64. Enabling/Disabling SPU Display via FSTA_DSP and STA_DSP Display Commands

***SPSwitch* (0x6C)**			
15 - 3		**2**	**1, 0**
reserved		SPSkip	SPDisplay
Reserved bits must be 0.			
SPSkip	0 = Reserved, do not use. 1 = Sub-pictures whose start time has already been passed by **SCLK** are displayed at least once.		
SPDisplay	00b = Reserved, do not use. 01b = Sub-picture is displayed on FSTA_DSP or STA_DSP sub-picture commands. 10b = Sub-picture is displayed on FSTA_DSP sub-picture commands only. 11b = Reserved, do not use.		

Bit 2 of the *SPSwitch*[1] parameter controls discarding of sub-picture units which are “late”. If bit 2 is equal to 1 the sub-picture decoder will process all SPUs for which the start time has already passed.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

NTSC <-> PAL Conversion: SPU Vertical Scaling

The *SPScale*[1] set-up parameter indicates if fixed vertical scaling is done on the sub-picture data to accommodate NTSC <-> PAL conversion as follows. All other combinations of *SPScale* are reserved and not to be used:

- *SPScale* = 0x0000, no vertical scaling of SPU.
- *SPScale* = 0x0001, vertical scaling is 5/6, scaling down PAL sub-picture for NTSC display.
- *SPScale* = 0x0002, vertical scaling is 6/5, scaling up NTSC sub-picture for PAL display.

SPScale only affects the scaling of the sub-pictures, not their position on the display. The following action is recommended when performing NTSC-to-PAL conversion where sub-pictures are involved:

- For menus or other bitstreams that make use of highlight information (see next sub-section), perform no scaling on the image and subpictures and center the 480 line NTSC image within the 576 PAL display lines with the *ActiveStartY*[1] and *ImageStartY*[1] set-up parameters.
- For bitstreams that use sub-pictures as subtitles and are letterboxed (as explained in Section 7. “Video Scaling and Panning”), the correct positioning of the subpictures on the display can be achieved by modifying *ActiveStartY* and *ImageStartY*.
- For bitstreams that use sub-pictures as subtitles and are not letterboxed, the subpictures will be shifted 6/5 upwards relative to their expected position.

6.8.3 Highlight (HLI) Processing

Highlight information (HLI) is part of a PCI packet, which is roughly one half of every NV_PCK. HLI is meant to temporarily highlight a selected rectangle of a sub-picture image. ‘Highlighting’ a rectangle means that the palette indices (color codes) and blending factors of the pixels in the specified rectangle are changed, according to the HLI. Only one rectangle can be highlighted at any given time. Highlight is displayed only when sub-picture is displayed. In the DVD terminology, a rectangle that has the potential of being highlighted is called a ‘button’.

The processing of a HLI block is shared between the **ZR36710** and the host. The host extracts the relevant Highlight information out of the effective HLI block in SDRAM as explained in Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”, packs it, and provides the **ZR36710** with the sufficient information to execute the highlighting tasks. This packed information is presented to the **ZR36710** as seven set-up parameters: *HiLightButton1, HiLightButton2, HiLightColor1, HiLightColor2, HiLightColor3, HiLightTiming* and *HiLightSwitch*[1].

The **ZR36710** handles the execution of highlighting the buttons, including dynamic switching between *HiLightButton1* and *HiLightButton2*.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.8.4 Highlight Parameters

The parameters are depicted in Figure 36. *HiLightButton1* and *HiLightButton2* may change during HLI display. The **ZR36710** holds a double buffer for these values. The data is read from one buffer while new parameters can be written to the other buffer. The buffers are changed whenever the *HiLightSwitch* parameter is written. *HiLightColor* and *HiLightTiming* can be changed only when Highlight is switched off. In general, *HiLightButton1, HiLightButton2, HiLightColor1, HiLightColor2, HiLightColor3* and *HiLightTiming*[1] contain geometrical (coordinates), color, and timing information for the buttons.

6.8.4.1 *HiLightButton1* and *HiLightButton2*

Each one of these parameters defines the geometrical position and appropriate color table of one button. They describe the locations of the upper-left and bottom-right pixels of a button. They are used as comparison values indicating locations where the SPU pixel data (PXD) decoding process should use the corresponding value provided by the selected *HiLightColor(1,2 or 3)* parameter.

The bit arrangement of these two parameters (see Figure 36) reduces host overhead in bit manipulation. The format is identical to that of the HLI data format as specified in the DVD Specifications 1.0.

6.8.4.2 HiLightColor1, HiLightColor2 and *HiLightColor3*

These parameters define two sets of palette indices (also called color codes) and blending factors. One set is denoted 'selection' set and the other one 'activation' set. When Highlight is executed, one of the sets (either the selection set or the activation set) is used within the geometrical boundaries of the highlighted button. The BTN_COLN bits of the *HiLightButton(1 and 2)* parameters indicate which one of these parameters is associated with the button. Valid values are 1, 2 or 3 for BTN_COLN.

6.8.4.3 *HiLightTiming*

This parameter defines three timing markers, HLI_S_PTM, HLI_E_PTM and BTN_SL_E_PTM, that describe three points in time (in units of the 90 KHz **SCLK**) that may be referred to by the *HiLightSwitch* parameter. HLI_S_PTM and HLI_E_PTM specify the start and end points (respectively) of the valid period of the Highlight function. No button is highlighted outside of this time window. BTN_SL_E_PTM indicates the expiration time of the period in which the DVD player waits for the user to select a button through its pointing device. The DVD specifications impose some limitations, which the **ZR36710** adheres to, that always apply for these three time markers:

- HLI_S_PTM < BTN_SL_E_PTM $\leq$ HLI_E_PTM.
- HLI_S_PTM = PTS of the SPU it is associated with.
- HLI_E_PTM = start time of the DCSQ, where an **STP_DSP** command exists.
  = PTS of the next SPU, if there is no **STP_DSP** command in this SPU.
  = 0xFFFFFFFF, in case of a still frame (e.g. menu file).

The host has to adjust these times by the same delay value used to adjust the PTSes of the SPUs (*VidPortDelay*[1] set-up parameter).

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

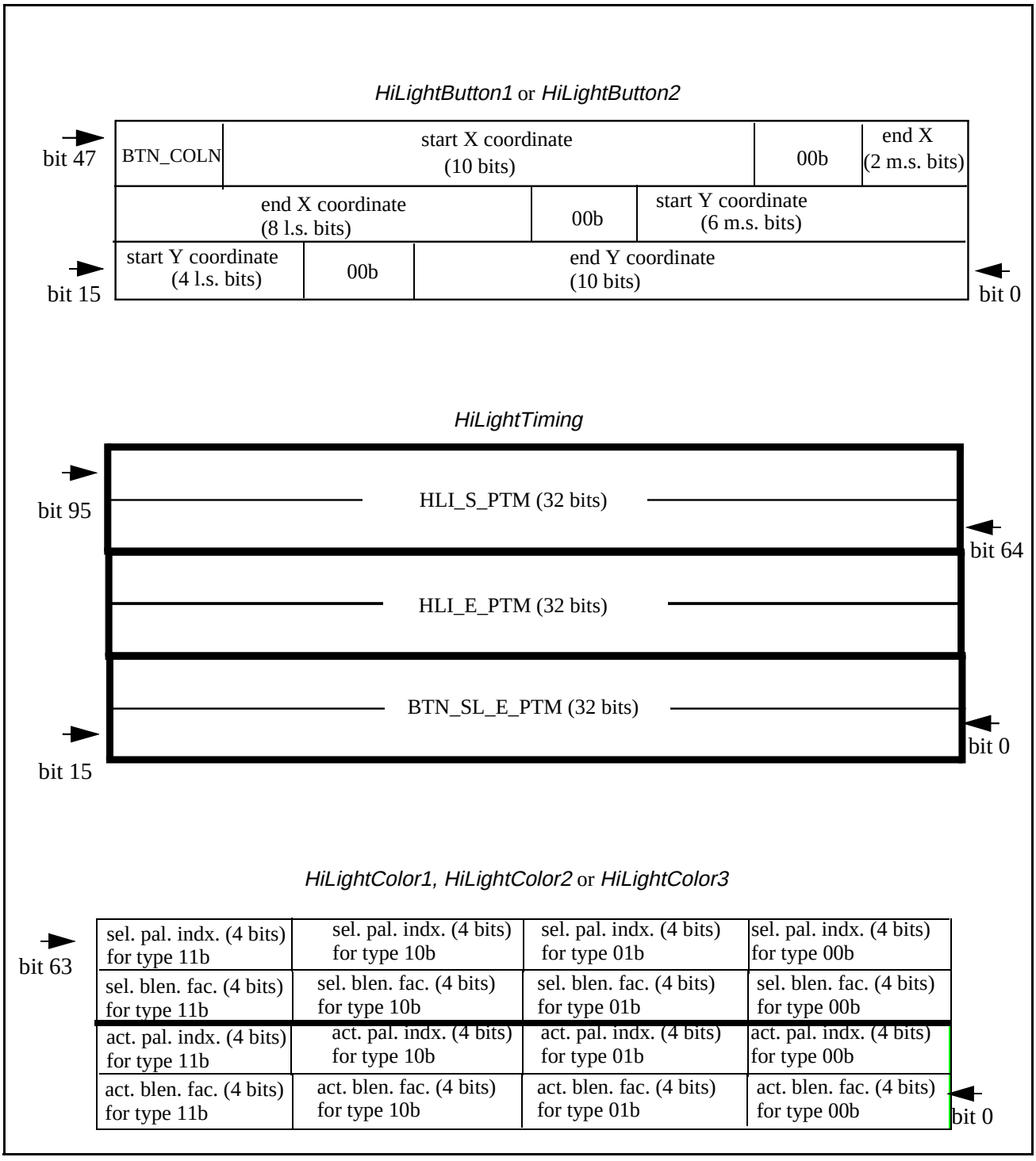

FIGURE 36. Structure of the Highlight parameters

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Phone (408) 919-4111 Fax (408) 919-4122

Indication of Relative Highlight Timing

The sub-picture decoder indicates the relative Highlight timing to the host, through the **HLI_TIME** bits of the **STATUS1**[1] register:

- **HLI_TIME** = 00b, HLI is disabled.
- **HLI_TIME** = 01b, the system time is between HLI_S_PTM and BTN_SL_E_PTM.
- **HLI_TIME** = 10b, the system time is between BTN_SL_E_PTM and HLI_E_PTM, or exactly at one of them.
- **HLI_TIME** = 11b, the system time, as determined by the system clock, is after the HLI_E_PTM time.

The indication of Highlight timing is meant to be used by the host in order to determine if a remote-control command sent by the user is valid and should be issued, or if it is out of the allowed time and should be ignored.

6.8.4.4 HiLightSwitch

When this parameter is written, the **ZR36710** switches reading button coordinates from one buffer of the *HiLightButton1* and *HiLightButton2*[2] double-buffers to the other and allows the host to write new values to the original buffer the device was reading from. This parameter specifies the sequential order by which the Highlight is to be executed. It covers all possible scenarios. The options are listed in Table 65 .

The following rules are associated with the *HiLightSwitch* parameter:

- There is no highlighting when sub-picture display is disabled.
- No more than one button can be highlighted (selected or activated) at any given time. Hence, when a new button is highlighted, the previously highlighted button is no longer highlighted (the original SPU is displayed without any hilighting).
- If the sub-picture stream ID is changed while Highlight is displayed, then Highlight is stopped and not resumed automatically, even when sub-picture display starts from the new stream, until a new HLI block appears in the new stream, is completely copied to the sub-picture code buffer in the SDRAM, and the host sends a new *HiLightSwitch* parameter with a value that invokes highlighting.
- In order to update Highlight parameters it is necessary to write the *HiLightSwitch* parameter (even with the same value as before). Once new Highlight parameters are written and updated by writing the *HiLightSwitch* parameter, the host must wait until the next effective edge of ***VSYNC*** before such an update is allowed again.

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.
2. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

TABLE 65. Interpretation of the *HiLightSwitch* parameter

Value	Meaning	Typical Application
0x0000	Disable the Highlight function now (all buttons return to default color codes and blending factors.	For stopping of Highlight (usually applied after an 'activation').
0x0001	Highlight Button 1, using the selection set, starting in HLI_S_PTM, until BTN_SL_E_PTM, then highlight Button 1, using the activation set, until HLI_E_PTM, then stop highlighting.	For the initial selection of a (default) button for the selection period, then, if no action was done by the user, activation of the already selected button.
0x0002	Highlight Button 1, using the selection set, starting now (but only if HLI_S_PTM has already passed), until BTN_SL_E_PTM, then highlight Button 1, using the activation set, until HLI_E_PTM, then stop highlighting.	For the selection of a (new) button for the (rest of the) selection period, then if no action was done by the user, activation of the already selected button.
0x0003	Highlight Button 1, using the selection set, starting in HLI_S_PTM, until BTN_SL_E_PTM, then highlight Button 2, using the activation set, until HLI_E_PTM, then stop highlighting.	For the initial selection of a (default) button for the selection period, then, if no action was done by the user, activation of the "forcedly activated" button.
0x0004	Highlight Button 1, using the selection set, starting now (but only if HLI_S_PTM has already passed), until BTN_SL_E_PTM, then highlight Button 2, using the activation set, until HLI_E_PTM, then stop highlighting.	For the selection of a (new) button for the (rest of the) selection period, then if no action was done by the user, activation of the "forcedly activated" button.
0x0005	Highlight Button 1, using the selection set, starting in HLI_S_PTM, until HLI_E_PTM, then stop highlighting. Important: See paragraph below this table.	For the initial selection of a (default) button for the selection period, then, if no action was done by the user, and no "forcedly activated" button is defined, stop highlighting.
0x0006	Highlight Button 1, using the selection set, starting now (but only if HLI_S_PTM has passed), until HLI_E_PTM, then stop highlighting. Important: See paragraph below this table.	For the selection of a (new) button for the (rest of the) selection period, then, if no action was done by the user, and no "forcedly activated" button is defined, stop highlighting.
0x0007	Highlight Button 1, using the activation set, starting now (but only if HLI_S_PTM has passed), until HLI_E_PTM (or a stop indication before that).	For the "direct" activation of a button, by a numerical key-pad user choice (as opposed to an arrow-based cursor plus an "ENTER" key).
0x0008	Highlight Button 2, using the activation set, starting now (but only if HLI_S_PTM has passed), until HLI_E_PTM (or a stop indication before that).	For the "direct" activation of a button, by a numerical user choice (as opposed to an arrow-based cursor plus an "ENTER" key).
0x0009 - 0xFFFF	reserved (no operation).	

HiLightSwitch = 0x0005 or 0x0006: Host Software Workaround

For *HiLightSwitch* = 0x0005 or 0x0006, the selection period is supposed to stop at BTN_SL_E_PTM. A bug in the **ZR36710** is the reason the selection period stops at HLI_E_PTM. Therefore, if the host writes 0x0005 or 0x0006 to *HiLightSwitch*, the host should periodically check (e.g. on every ***VSYNC*** interrupt) for **HLI_TIME** = 10b in the **STATUS1**[1] register and once the host reads this value, the host writes 0x0000 to *HiLightSwitch* to achieve the intended functionality.

1. See Section 5.5 "Status Registers - Reg. 0x3, 0x4, 0x5 (Read)" for an explanation on reading status register bits.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.9 Error Indication and Concealment

For the cases of DVD and VideoCD playback (*CBSelect*[1] = 00000b or 00010b), the **ZR36710** can indicate errors to the host through the **STATUS2** register as shown in Table 66 .

TABLE 66. Error indication in STATUS2 register

Bit #	Error Type	Indication
14	Video error	0 = no error 1 = error
13	System demultiplexing error	0 = no error 1 = error

Error concealment that can be performed on DVD or VideoCD video content can be set through bit 7 of *DVPGen2*[1], but all other bits of this general DVP input parameter must be left as they were. Other bits are used for other purposes (e.g. NV_PCK retrieval method) and should not be changed. This bit has the following functionality:

TABLE 67. Selecting the video error concealment via *DVPGen2* bit 7

***DVPGen2* (0x04)**		
15 - 8	**7**	**6 - 0**
*	Concealment	*
* = Bits used for other functions that must be left as they were.		
Concealment	0 = At Macroblock (MB), slice and picture levels. May cause more freezes, but less green blocks. 1 = At MB and slice levels. May cause less freezes, but more green blocks.	

6.10 A/V Synchronization

The synchronization between audio, video and sub-picture data is handled within the **ZR36710**, requiring no host intervention other than initialization of the synchronization parameters. In summary, the **ZR36710** supports two types of A/V synchronization: “clock master” and “audio master”. The type of synchronization used is determined by set-up parameter settings. A third type of synchronization is also offered, “no synchronization”, in which both the video and audio decoders do not synchronize to any clock.

Clock Master A/V Sync

The **ZR36710** has an internal system clock counter (programmed to 90KHz) that is used to compare with video DTS and audio PTS values. If the discrepancy between the video DTS and internal system clock is too large, a video frame is either dropped or repeated for one frame period in order to closer

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

match the next video DTS to the system clock. If the discrepancy between the audio PTS and system clock is too large, an audio frame is either dropped or paused for one frame period in order to closer match the next audio PTS to the system clock.

Audio Master A/V Sync

To avoid any audible artifacts caused by repeating or pausing audio frames, the ADP is allowed to decode audio at it's desired rate, as long as there is data in within the audio SDRAM buffer. The ADP retrieves PTS values from the audio stream and writes these values to the system clock counter. The video decoding process will synchronize to the system clock counter in the same manner it would with clock master A/V sync.

For bitstreams that are encoded under the guidelines imposed for MPEG-1 (ISO 11172-1), MPEG-2 (ISO 13818-1) or DVD where the video and audio clocks used during encoding were locked, neither of these synchronization schemes will be needed (with minor exceptions for SCR gaps during seamless play (DVD playback), code FIFO starvation by the system, or a change in stream IDs during playback). This requires that ***GCLK*** is locked to ***GCLK1*** and the PLL parameters are configured appropriately as explained in Section 4.2 "Phase-Locked Loop Interface".

The functional blocks of the synchronization mechanism are explained in the following sub-sections.

6.10.1 Internal SCLK Counter

The **ZR36710** has an internal 32-bit system clock counter, **SCLK** that increments in units of 90KHz. This clock is the primary clock used for synchronization purposes. **SCLK** is derived from ***PCLK*** as follows:

- **SCLK** = ***PCLK*** / 900, ***PCLK*** must be 81MHz.

If ***GCLK*** = 27 MHz, *DSPM*[1] and *DSPD*[1] are left at their default values after RESET, then **SCLK** = 81MHz / 900 = 90 KHz.

Initialization and Operation of SCLK

SCLK must be initialized at the start of decoding. The DVP will automatically initialize **SCLK** to the first SCR encountered in the bitstream without any host intervention. Prior to this initialization, **SCLK** remains 0x00000000. Once this initialization takes place, the **SCLK** counter begins counting in clock master mode. Writing the appropriate parameter to the PARAM (EXT = 0x03)[2] ADP command (as shown in Table 68) will determine whether **SCLK** will continue to count in clock master mode or in audio master mode.

1. See Section 12.4 "Set-up Commands" for an explanation on ***PCLK*** parameters via ADP commands.
2. See Section 12.4 "Set-up Commands" for an explanation on setting the A/V sync mode in the ADP.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

The host has the option of re-initializing **SCLK** to the next SCR encountered in the bitstream. This is done by writing to the *Vlock* bit of the *VidSyncMode*[1] set-up parameter as shown in Table 69 . However, if a bitstream contains SCR discontinuities, the *Vlock* bit should not be toggled from 0 to 1. Handling SCR discontinuities are explained further in Section 6.10.5 “Handling SCR Discontinuities”.

TABLE 68. Determining Clock Master or Audio Master

PARAM (EXT = 0x03) - Audio Synchronization with SCLK	
PARAM (EXT = 0x03) (2-byte parameter)	0x0000 = Audio does not synchronize to **SCLK** counter. (no sync). 0x0001 = Audio synchronizes to **SCLK** counter (clock master mode). 0x0002 = **SCLK** synchronizes to timestamps in audio stream (audio master mode). 0x0003 = On next frame, audio syncs to **SCLK** (clock master) and then changes to audio master mode.

TABLE 69. Vlock bit - Setting SCLK to the first SCR in Bitstream

***VidSyncMode* (0x48)**		
15 - 2	**1**	**0**
reserved	Vlock	VsyncMode
Reserved bits must be 0.		
Vlock	0 = no functionality. 1 = The transition of setting this bit from 0 to 1 causes **SCLK** to initialize to the next SCR in the bitstream. This can only be done between the **start** and **end_playback** host commands to take effect. This bit may remain 1 and have no effect. Once this bit is cleared, the next transition to 1 will cause **SCLK** to reinitialize to the next SCR in the bitstream.	
VsyncMode	0 = Video does not synchronize to **SCLK** counter. 1 = Video synchronizes to **SCLK** counter.	

SCLK is stopped while the decoding is put into the ***Pause*** state by one of several host commands as explained in Section 6.11 “Host Commands and Control over the Playback Operation”. **SCLK** continues counting once the decoding resumes from the ***Pause*** state by calling one of several host commands.

SCLK continues to count after playback has been stopped by an **end_playback**[2] host command. **SCLK** is stopped if playback stops because an MPEG system end code is encountered in the bitstream. It will be reinitialized once playback is restarted with the next **start**[2] host command.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 6.11 “Host Commands and Control over the Playback Operation” for an explanation on writing host commands to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

Reading the Value of SCLK

At any time, the host can retrieve the current value of **SCLK** by reading the System Clock Register as explained further in Section 5.9 “Reading the System Clock Counter - Reg. 0x9 (Read)”. If the bitstream contains SCR discontinuities, the value read back will not match the timestamp of the currently-displayed frame. See Section 6.10.5 “Handling SCR Discontinuities” for further details on how SCR discontinuities are handled.

Interrupt on SCLK

The host can designate a value of **SCLK** that will trigger an interrupt to the host. This interrupt is available as an added feature for a system design, such as a “sleep” mechanism in which a player is turned off automatically after **SCLK** counts for an hour. This interrupt is configured by writing a value to the *SCLKValue*[1] set-up parameter which indicates what value of **SCLK** triggers the interrupt and by clearing the **SCLKIRQ** bit in the IMR[2].

6.10.2 Video Synchronization

Table 69 shows how the *VsyncMode* bit of the *VidSyncMode*[1] set-up parameter determines whether or not video will synchronize to **SCLK**. If the host determines that video does not synchronize to **SCLK**, then the **ZR36710** decodes and displays every video frame within the video code buffer in SDRAM. If the host determines that video must synchronize to **SCLK**, then the following explains how video synchronization is handled within the device. The *VsyncMode* bit can change during playback, so the host can enable and disable video synchronization to **SCLK** randomly during playback.

Setting *VidPortDelay*

During demultiplexing of the bitstream and transfer of the video data to the video code buffer in SDRAM, the **ZR36710** will not only copy the video stream, but also copy the PTS and DTS values of frames that have such values associated with them. These timestamps are modified by the *VidPortDelay*[1] set-up parameter.

The *VidPortDelay* parameter designates an offset to be added to the timestamps. This value is in units of **SCLK**. This value is used to correct any constant offset between the video and audio due to their reconstruction chains in which the presentation of the video precedes the presentation of the audio. If the video trails the audio, then this value should be 0. This value must be initialized prior to decoding and can not change during playback of video.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on setting IMR bits.

Adding Constant Offset to Video DTS for VideoCD Playback

In VideoCD playback (*CBSelect*[1] = 00000b), another constant offset may be added by the ADP to the DTS value for each frame. This offset may be needed to compensate for a clock mismatch in case bitstream is provided via the CD-DSP interface and the CD-DSP interface's clock is not locked to the clocks (***GCLK*** and ***GCLK1***) of the **ZR36710**. The value of this offset is fixed in the VideoCD playback microcode (e.g. 0.7 seconds) and is indicated in the microcode release notes.

Discarding or Repeating Video Frames for A/V Sync

The video decoder waits for **SCLK** to reach the initial video DTS before it starts to decode. Whenever the video decoder encounters a timestamp, it compares the timestamp value with the current value of **SCLK** prior to decoding the frame.

For the frame to be considered synchronized to **SCLK**, the difference between the timestamp and **SCLK** must fall within a tolerance that is specified by the *VidTolerance*[1] set-up parameter. The host can change the value of *VidTolerance* at any time before and during playback. *VidTolerance* is measured in units of **SCLK**. If the following condition is met, the picture to be decoded is considered synchronized, is decoded and displayed:

- **SCLK** - *VidTolerance* <= timestamp <= **SCLK** + *VidTolerance*, good synchronization.

If the video is "ahead" of **SCLK**, then decoding of video needs to be paused for one frame period until **SCLK** "catches up" and the two are synchronized once again. While decoding is paused for one frame period, the current displayed frame is displayed for an extra frame period. It may be necessary to pause decoding on several frames until the video and **SCLK** are synchronized. This condition occurs when:

- timestamp > **SCLK** + *VidTolerance*, video must be paused until **SCLK** catches up.

If the video is "behind" **SCLK**, then a video frame needs to be discarded and decoding would resume with the following frame until the timestamp "catches up" with **SCLK** and the two are synchronized once again. The **ZR36710** will discard only B-pictures (MPEG-1) or B-frames (MPEG-2, only B-frames whose "repeat_first_field" flag = 0) and never discard two consecutive frames. Several B-frames may need to be discarded until the video and **SCLK** are synchronized. This condition occurs when:

- timestamp < **SCLK** - *VidTolerance*, B-frame must be skipped until timestamp catches up.

6.10.3 Audio Synchronization - Clock Master Mode

If the ADP is configured for audio master mode, the ADP will not need to perform any audio synchronization to **SCLK** because the PTS values within the audio stream determine the value of **SCLK** (in essence, audio is always synchronized to **SCLK**). However, if the audio playback is operating in clock master mode, then the ADP can be configured to perform audio synchronization to **SCLK**. Table

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

68 shows how the PARAM (EXT = 0x03) ADP command determines whether or not audio will synchronize to **SCLK**. If the host determines that audio does not synchronize to **SCLK**, then the **ZR36710** decodes and outputs every audio frame within the audio code buffer in SDRAM. If the host determines that audio must synchronize to **SCLK**, then the following paragraphs explain how audio synchronization is handled within the device. The host can change the 2-byte parameter of the PARAM (EXT = 0x03) ADP command between the 0x0000 and 0x0001 settings at any time before or during playback so audio synchronization to **SCLK** can be enabled or disabled randomly by the host.

Setting *AudPortDelay*

During demultiplexing of the bitstream and transfer of the audio data to the audio code buffer in SDRAM, the **ZR36710** will not only copy the audio stream, but also copy the PTS values of frames that have such values associated with them. These timestamps are modified by the *AudPortDelay*[1] set-up parameter.

The *AudPortDelay* parameter designates an offset to be added to the timestamps. This value is in units of **SCLK**. This value must be initialized prior to decoding and can not change during playback. This value is used to correct any constant offset between the audio and video due to their reconstruction chains in which the presentation of the audio precedes the presentation of the video. If the audio trails the video, then this value should be 0.

Adding Constant Offset to Audio PTS for VideoCD Playback

In VideoCD playback (*CBSelect*[1] = 00000b), another constant offset may be added to the PTS value for each audio frame. This offset may be needed to compensate for a clock mismatch in case bitstream is provided via the CD-DSP interface and the CD-DSP interface's clock is not locked to the clocks (***GCLK*** and ***GCLK1***) of the **ZR36710**. The value of this offset is fixed in the VideoCD playback microcode (e.g. 0.7 seconds) and is indicated in the microcode release notes.

Discarding or Repeating Audio Frames for A/V Sync

The ADP waits for **SCLK** to reach the initial audio PTS before it starts to output the decoded audio. Whenever the ADP encounters a timestamp, it compares the frame's PTS value with the current value of **SCLK** prior to decoding.

For the frame to be considered synchronized to **SCLK**, the difference between the PTS and **SCLK** must fall within a tolerance that is specified by the 2-byte parameter of the PARAM (EXT = 0x02)[2] ADP command. This tolerance is measured in units of **SCLK**. The host can change this value any time before or during playback.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 12.4 "Set-up Commands" for an explanation on setting audio sync tolerances within the ADP.

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Phone (408) 919-4111 Fax (408) 919-4122

If the following condition is met, the frame is considered synchronized and the frame is output:

- **SCLK** - tolerance <= PTS <= **SCLK** + tolerance, good synchronization.

If the audio is "ahead" of **SCLK**, then output of audio needs to be paused and muted for one frame period until **SCLK** "catches up" and the two are synchronized once again. It may be necessary to pause the output on several frames until the audio and **SCLK** are synchronized. This condition occurs when:

- PTS > **SCLK** + tolerance, audio must be paused and muted until **SCLK** catches up.

If the audio is "behind" **SCLK**, then an audio frame needs to be discarded until the PTS "catches up" with **SCLK** and the two are synchronized once again. Several audio frames may need to be discarded until the audio and **SCLK** are synchronized. This condition occurs when:

- PTS < **SCLK** - tolerance, audio frame must be skipped until PTS catches up.

6.10.4 Sub-picture and HLI Synchronization

As explained in Section 6.8 "Sub-Picture Decoding with HLI Support", the sub-picture decoder and HLI processor of the **ZR36710** automatically handle decoding and display of SPUs and HLI.

6.10.5 Handling SCR Discontinuities

SCR discontinuities are defined for DVD bitstreams (*CBSelect*[1] = 00010b) as seamless, non-seamless and still. The **ZR36710** can handle seamless discontinuities that allow for seamless playback without any need to stop the decoding process with an **end_playback**[2] host command. To handle non-seamless and still discontinuities, the host must issue **end_playback** and **start**[2] host commands.

Note that during I-only playback mode (i.e. fast forward/fast backward as explained in Section 6.11.6 "Host Command: fast_search") the timestamps in the bitstream are ignored so discontinuities are also ignored.

To handle discontinuities, the **ZR36710** has an internal 32-bit variable **GLOBAL_DELTA**. When a discontinuity is encountered in a new VOBU, **GLOBAL_DELTA** is calculated as the difference between the SCR at the end of the previous VOBU and the newly-encountered SCR of the current VOBU. **GLOBAL_DELTA** is added to any timestamp found in the video, audio and sub-picture packets. Note that the timestamps are modified, but **SCLK** remains unchanged.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 6.11 "Host Commands and Control over the Playback Operation" for an explanation on writing host commands to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

GLOBAL_DELTA can be provided to the host via the DVP Data Register as explained in Section 5.6.2 “Reading Data from the DVP Data Register”. The data format is as follows:.

TABLE 70. SCR Discontinuity Data Format to Host

	15 - 14	13 - 7	6 - 0
Tag Word	01b	0000010b	0000101b
parameter 1	m.s. word of GLOBAL_DELTA		
parameter 2	l.s. word of GLOBAL_DELTA		

6.11 Host Commands and Control over the Playback Operation

Control over the playback operation by the host is done through issuing host commands via the Host Command Register as explained in Section 5.3 “Issuing Host Commands - Reg. 0x3 (Write)”. Each host command is 16 bits in the following format:

- m.s. byte is the “op-code” byte.
- l.s. byte is the command parameter byte.

The list of the host commands including the values of the op-code byte and parameter byte is given in the table below. All other combinations are reserved.

TABLE 71. Host Commands

Op-Code (m.s. byte)	Command parameter	Description
0x00	00000 000b	**start** - Start or restart normal speed playback
0x01	00000 000b	**pause_stream**
0x03	00000 000b	**single_stepping**
0x05	00000 SSSb	**slow_motion** with factor 2 to 7
0x07	00000 00Eb	**end_playback**
0x08	00000 FFFb	**fast_search**
0x09	00000 000b	**continue** normal speed playback
0x0E	00000 000b	**sequence_end_code** - display last decoded pictures

The **HCRDY** bit of the **STATUS1**[1] register indicates when the host can send host commands to the device. When this bit is high, the Host Command Register is empty and the next host command can be sent to the **ZR36710**. **HCRDY** low indicates that the Host Command Register is not empty so the next host command should not be sent to the **ZR36710**. If a host command is written to the **ZR36710** while

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

the Host Command Register is not empty, it will overwrite the host command currently residing in the register.

6.11.1 Operation States of the ZR36710

The **C-STATE** bits of the **STATUS0**[1] register indicate the playback and non-playback states of the **ZR36710** as shown in Table 72 .

TABLE 72. Playback and Non-Playback states of the **ZR36710**

STATUS0 Register (Read Register 0x3)										
15 - 10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C-STATE	reserved	DRAMBE	DRAMBF	VCBE	VCBF	ACBE	ACBF	SPCBF	ADPEMPTY	ADPRDY
Reserved bit values must be ignored by system since value is undefined.										
C-STATE	Internal operating state. Several of these states are reflective of the last host command issued to the device. Allowed values are as follows: 00 0000b = ***reset*** state: The period between RESET and locking of ***PCLK*** by the PLL circuitry. 00 0010b = ***init_pclk*** state: The period while ***PCLK*** is locked, but the *StartDisplay*[a] parameter has not been given. 00 0011b = ***init_display***: The period after *StartDisplay* has been given, but prior to a **start** host command. 01 0000b = ***Pause*** (active video) state: Playback is paused with the output of a frame. 01 1000b = ***Pause*** (no active video) state: Playback is paused with no decoding/display of a frame. 10 0000b = ***Nspb*** (active video) state: Non-stop playback with the output of a frame. 10 1000b = ***Nspb*** (no active video) state: Non-stop playback with no decoding/display of a frame. 10 0011b = ***Step*** (active video) state: Single-step playback. 10 1011b = ***Step*** (no active video) state: Single-step playback. 10 0101b = ***Slow*** (active video) state: Slow-motion playback. 10 1101b = ***Slow*** (no active video) state: Slow-motion playback. 11 0000b = ***Idle*** state: Period between end of decoding and next **start** host command. All other combinations are reserved and must not be used.										

a. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

The transition between states is accomplished by either the execution of a host command or is handled automatically by the **ZR36710** at the appropriate time. Figure 37 is a state diagram that illustrates the relationship between state transitions and host commands.

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

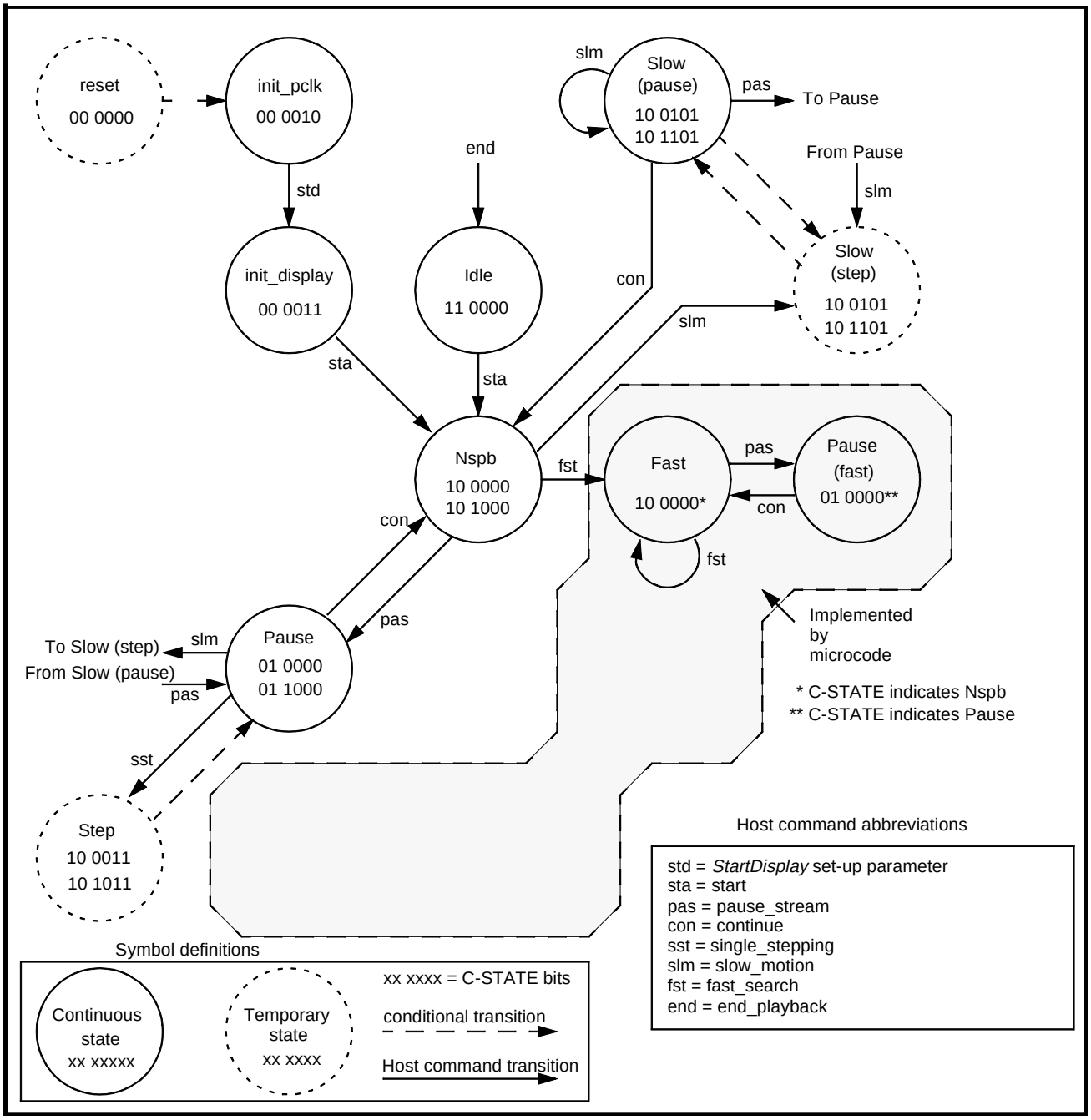

FIGURE 37. ZR36710 State Transition and Host Command Diagram

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6.11.1.1 Transitions Between Non-Playback and Playback States

The ***reset***, ***init_pclk***, ***init_display*** and ***Idle*** states are the non-playback states of the device. All other states are the playback states. As indicated in Figure 37, a **start** host command from either the ***init_display*** or ***Idle*** states puts the device into playback mode as explained throughout this section.

Once in a playback state, the device will return to the ***Idle*** state on either of the following conditions:

- An "MPEG_program_end_code" (0x000001B9) is parsed by the DVP.
- The host issues an **end_playback** host command. The response of the device to this command is explained in Section 6.11.5 "Host Command: end_playback".

6.11.1.2 Executing Host Commands from Continuous and Temporary States

While the device is in a continuous state, the **ZR36710** checks the host command register once every frame period (for MPEG-2) or picture period (for MPEG-1) before starting to decode the next frame (if video is present). If the decoding of the next frame is delayed (e.g. 3/2 pulldown), the check of the host command register is also delayed by the same time interval. If the host command register is empty, the **ZR36710** continues to operate in the same state as before.

Figure 37 indicates which host commands may be executed from each state of operation. The **ZR36710** will discard any host commands that are not allowed to be executed from the current state of operation. Once a host command is executed by the **ZR36710**, the command is removed from the register. The **start** host command will cause incorrect functionality once the device is in playback so this host command must not be sent by the host while the device is not in the ***Idle*** or ***init_display*** states.

While the device is in a temporary state, **HCREADY** will indicate that no host commands should be issued to the **ZR36710** with the exception of **end_playback** in which playback is immediately terminated and the device is returned to the ***Idle*** state. If the temporary mode is allowed to continue without termination by an **end_playback** command, the **ZR36710** will automatically complete the operation of the temporary mode and change to the ***Pause*** state.

6.11.1.3 Allowed Host Commands for Non-Video Bitstreams

If there is no video stream decoded (bit 13 of **STATUS0**[1] register = 1), the allowed commands are **pause_stream**, **single_stepping**, **slow_motion** and **continue** while the device is in the ***Nspb*** state.

6.11.1.4 Allowed Host Commands if No Bitstream Transfer Takes Place

If the **ZR36710** is configured to decode video, once the **start** host command is given the **ZR36710** will only respond to the **end_playback** command until a video sequence header is encountered (if video is present). All other host commands will be discarded. This allows the host to put the device into the ***Idle*** state without transferring any bitstream to the device after having issued a **start** command.

1. See Section 5.5 "Status Registers - Reg. 0x3, 0x4, 0x5 (Read)" for an explanation on reading the status register bits.

6.11.2 Host Command: pause_stream

After the **ZR36710** receives the **pause_stream** host command (op-code 0x01), the device will suspend decoding of the next frame and switch to the ***Pause*** state. Audio decoding is stopped. Audio output is frozen and muted. The video output freezes on the last displayed frame. The **SCLK** counter is stopped. The next (allowed) host command will be executed one frame period after the **ZR36710** went into the ***Pause*** state, if a host command is pending execution in the Host Command Register.

The fixed scaler in the video processing unit (see Section 7.2 “Fixed Scaling to CCIR601-Size Interlaced Display Frames”) does field interpolation as an alternative to displaying two fields of video that may not represent the same instance of time and show artifacts. However, the field interpolation can be disabled as explained in Section 7.2 “Fixed Scaling to CCIR601-Size Interlaced Display Frames”.

Sub-picture output is frozen automatically by the stopping of the **SCLK** counter. The closed-caption output will make use of the value in the *CaptionWord*[1] set-up parameter. This value should be initialized to the NOP character (0x0000) prior to playback, causing the closed-caption output to be paused while the device is in the ***Pause*** state. OSD and HLI data can be changed while in the ***Pause*** state. Changes to these will adjust the display accordingly.

If the system wants to pause the display on a particular frame, the host needs to observe ***VSYNC*** interrupts[2] and the **PICTYPE** bits of the **STATUS1**[3] register.

Once a **continue** host command (op-code 0x09) is received, the **ZR36710** will switch to the ***Nspb*** state and resume its normal speed playback operation by decoding of the next frame and restarting decoding and output of audio. If the audio was muted with a MUTE ADP command, it is necessary to unmute the audio with an UNMUTE ADP command. The next (allowed) command will be executed one frame period after the **ZR36710** responds to the **continue** host command, if a host command is pending execution in the Host Command Register.

When the bitstream is coming from a DVD-DSP or CD-DSP, pausing the DVD (or CD) drive and starting to playback again may affect the average bit rate (depending on the size of the track buffer in the DVD-DSP/CD-DSP device) and delay the observable response to the **continue** command.

6.11.3 Host Command: single_stepping

After the **ZR36710** receives the **single_stepping** host command (op-code 0x03), the devices switches to the ***Step*** state. In this state, the **ZR36710** will decode the next frame (if video is present) then return to the ***Pause*** state. The ADP decodes audio, so it is recommended that the host issue a MUTE ADP command prior to issuing this host command in order to mute the output. ADP commands cannot be issued to the **ZR36710** while the device is in the ***Step*** state. The next (allowed) command will be executed one frame period after the **ZR36710** switched to the ***Pause*** state, if a host command is pending execution in the Host Command Register. Once paused, sub-picture output is frozen by the stopping of

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.
3. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading the status register bits.

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Phone (408) 919-4111 Fax (408) 919-4122

SCLK and closed-caption output is frozen by insertion of the NOP (0x0000) character to the *CaptionWord*[1] parameter.

6.11.4 Host Command: slow_motion

After the **ZR36710** receives the **slow_motion** host command (op-code 0x05, parameter 00000 SSSb, 'SSS' unsigned integer), the device switches to the ***Slow*** state. In this state, the **ZR36710** will repeatedly decode a single frame (if video is present), wait for ('SSS' - 1) frame periods, decode the next frame (if video is present), wait for ('SSS' - 1) frame periods, etc. The next (allowed) command will be executed one frame period after the **ZR36710** changes the displayed frame (if video is present), if a host command is pending execution in the Host Command Register. The ADP continues to decode audio so it is recommended that the host issue a MUTE ADP command prior to issuing this host command in order to mute the audio. ADP commands cannot be issued to the **ZR36710** while the device is in the ***Slow*** state.

When the bitstream is coming from an DVD-DSP/CD-DSP, pausing the DVD (or CD) drive and starting to playback again may affect the average bit rate and (depending on the size of the track buffer in the DVD-DSP/CD-DSP device) the effective slow-down factor.

After the next **pause_stream** command is received, or if a video sequence end code was detected, the **ZR36710** will go to the ***Pause*** state. Once paused, sub-picture output is frozen by the stopping of **SCLK** and the closed-caption output will make use of the value in the *CaptionWord* set-up parameter. This value should be initialized to the NOP character (0x0000) prior to playback, causing the closed-caption output to be paused while the device is in the ***Pause*** state.

6.11.5 Host Command: end_playback

After receiving the **end_playback** command (op-code 0x07, parameter 01000 00Eb), the **ZR36710** will terminate decoding after decoding the current picture (MPEG-1) or current frame (MPEG-2).

After termination, if E = 0 the device will continue to display the last displayed frame. If E = 1 the device will display the background color (specified by the *ColorY*, *ColorU* and *ColorV*[1] set-up parameters). The **ZR36710** will activate the ***IDLE*** signal and will switch to the ***Idle*** state.

The video sequence parameters which are used by the **ZR36710** are reserved for the next bitstream playback in case that they will be needed. This is necessary in case the video entry point for the next video stream is an I-picture and not its sequence header.

Audio decoding is stopped and the output muted. OSD continues its regular operation. For DVD bitstreams, sub-picture and HLI decoding stops and sub-picture display is switched off. Closed captions decoding stops and the *CaptionWord* is inserted.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.11.6 Host Command: fast_search

Fast search is a mode of operation in which the **ZR36710** discards just B-frames or both B- and P-frames and displays the remaining frames, achieving a speed-up effect. This mode is typically enabled when a DVD player is in “fast forward” or “fast reverse” modes. As with all modes of operation, fast search functionality is dependent on the DVP microcode that gets loaded prior to the **start** host command. Some versions of DVP microcode will support both normal speed playback and fast search modes. Other versions will have normal speed playback in one microcode, but will have fast search support in a separate microcode. Refer to the microcode release notes as to what features are supported in the microcode. If the microcode being used supports both normal speed playback and fast search modes, then the **fast_search** command as explained in this section is used. If normal speed playback and fast search are separated into separate microcodes, refer to Section 6.12 “Fast Search in DVD Using Dedicated DVP Microcode”.

Fast search for VideoCD is also a separate mode of operation that does not fall under the scope of this host command. For details on how to execute the fast search mode for VideoCD playback, please refer to Section 6.13 “Fast Search in VideoCD”.

After the **ZR36710** receives the **fast_search** host command (op-code 0x08, parameter 00000 FFFb, FFF = 000b is forbidden, 101b <= FFF <= 111b is reserved), the device switches to the ***Fast*** state (reflected on the **C-STATE** bits as the ***Nspb*** state as shown in Figure 37). In this state, the device discards all non-video streams and mutes the audio output. For DVD bitstreams, the device will stop decoding of sub-picture and HLI and switch off the sub-picture display. Closed captions data will not be decoded and the *CaptionWord*[1] inserted instead. The **ZR36710** will continue to output the OSD data.

As long as a video sequence end code is not detected, the **ZR36710** either copies complete pictures (MPEG-1) or frames (MPEG-2) to the video code buffer or discards them according to the ‘FFF’ value. Sequence and GOP headers (and the appropriate extensions for MPEG-2) are not discarded. The device continues to decode and display the coded video data in the SDRAM as if in normal speed playback.

- FFF = 001b, approximately every other picture (MPEG-1) or frame (MPEG-2) is discarded. All I and P-frames and some of the B-frames are decoded and displayed.
- FFF = 010b, all B-frames are discarded. All I and P-frames are decoded & displayed.
- FFF = 011b, all B and P-frames are discarded. All I-frames are decoded & displayed.
- FFF = 100b, Only I-frames are decoded and displayed, but the host does not have to provide a continuous bitstream. The host decides which portions of the bitstream to transfer to the **ZR36710**. Each portion must contain a complete I-frame.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

A “speed up” effect is achieved in this scheme. The actual speed-up ratio and its stability depend very much on the following factors:

- The speed-up factor that can be achieved in bitstream data transferred to the **ZR36710**.
- The arrangement of the various picture types in the video sequence and the sizes of the code of the various coded pictures.
- The display period of each frame in units of **SCLK**/256 as defined in Section 6.12.1 “I-Only Mode”.

Note:

- Synchronization with **SCLK** is suspended.

To stop the fast search, an **end_playback** host command is needed or an MPEG system end code is encountered in the bitstream by the DVP.

6.11.7 Host Command: sequence_end_code

Some DVD bitstreams do not have a video sequence_end_code after the last coded picture and because of this, the **ZR36710** will behave as if it is starving and not display some of the pictures in its picture buffers until it receives more pictures. To force the display of the pictures in the picture buffers in this situation, the host issues the **sequence_end_code** command (op-code 0x0E) after having sent all the data to the device.

6.12 Fast Search in DVD Using Dedicated DVP Microcode

If the DVP microcode supports both normal speed playback and fast search modes, then fast search is enabled by issuing a **fast_search** host command as explained in Section 6.11.6 “Host Command: fast_search”. This sections explains how fast search is handled if separate DVP microcodes are required for normal speed playback and fast search modes.

There are two types of fast search:

- I-Only mode in which the host provides only portions of the bitstream that contain complete I-frames.
- I & P mode in which the host provides the whole bitstream, but the B-frames are discarded.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

6.12.1 I-Only Mode

Table 73 shows the steps involved in I-Only mode operation.

TABLE 73. Protocol for I-Only Fast Search Mode (DVD)

I-Only Fast Search Mode for DVD Bitstreams
Step 1: Wait unitl **IDLE** = 1 in the **STATUS1** register. This can be achieved by issuing an **end_playback** command or resetting the device if it is not in the ***Idle*** state.
Step 2: Load the fast search DVP microcode.
Step 3: Clear bits 5 and 4 of *DVPGen2*, but keep all other bits of this general DVP input parameter the same as they were. Other bits are used for other purposes (e.g. NV_PCK retrieval method) and should not be changed.
Step 4: Determine the amount of time that each I-frame should be displayed and write this value to *DVPGen1*. The equation for determining this value is as follows: *DVPGen1* = int[(time in 90KHz units / 256)] For example, if the host wishes to display each picture for 200ms, then the equation becomes: *DVPGen1* = int[(90000 * 0.2) / 256)] = 71
Step 5: Issue the **start** command.
Step 6: The host must send sectors from the beginning of a VOBU. The NV_PCKs are retrieved by the device as they would be during normal speed playback. The **ZR36710** expects to receive the complete I-frame data. Extra sectors will be discarded, but the host must stop bitstream transfer after the last sector in which the I-frame resides. The host then seeks to the start of the next VOBU that contains the next I-frame to display.
Step 7: Repeat step 6 as often as necessary, depending on how many I-frames are to be displayed.
Step 8: Stop the I-Only mode by issuing an **end_playback** command.

6.12.2 I & P Mode

Table 74 shows the steps involved in I & P mode operation.

TABLE 74. Protocol for I & P Fast Search Mode (DVD)

I & P Fast Search Mode for DVD Bitstreams
Step 1: Wait unitl **IDLE** = 1 in the **STATUS1** register. This can be achieved by issuing an **end_playback** command or resetting the device if it is not in the ***Idle*** state.
Step 2: Load the fast search DVP microcode.
Step 3: Clear bit 5 and set bit 4 (01b) of *DVPGen2*, but keep all other bits of this general DVP input parameter the same as they were. Other bits are used for other purposes (e.g. NV_PCK retrieval method) and should not be changed.
Step 4: Issue the **start** command.
Step 5: The host sends the entire bitstream to the **ZR36710**. The device will display only the reference pictures. Of course for a speed-up effect to be seen, the DVD drive must support the higher bitrate necessary.
Step 6: Stop the I & P mode by issuing an **end_playback** command.

6.13 Fast Search in VideoCD

Fast search for VideoCD playback is similar to DVD I-Only mode fast search as explained in the previous section. Table 75 shows the steps involved in VideoCD fast search mode operation. This table shows the extra steps required if bitstream is provided via the CD-DSP interface and these extra steps are

explained in more detail in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”. If the bitstream is transferred via the host interface, these extra steps must be discarded.

TABLE 75. Protocol for VideoCD I-Only Fast Search Mode

I-Only Fast Search Mode for VideoCD Bitstreams
Step 1: Wait unitl **IDLE** = 1 in the **STATUS1** register. This can be achieved by issuing an **end_playback** command or resetting the device if it is not in the ***Idle*** state.
Step 2: Load the VideoCD DVP microcode (if not already loaded).
Step 3: Indicate which sectors to play by writing the start and end sector addresses to the DVP input FIFO as explained in Section 5.6.1 “Writing Data to the DVP Data Register”. This step is only necessary if data is passed via the CD-DSP interface and is explained in more detail in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”.
Step 4: Issue the **start** command.
Step 5: The host seeks within the bitstream to the start of a desired I-picture to display and feeds this to the **ZR36710**. If bitstream is via the CD-DSP interface, sectors are discarded until the start sector address is encountered.
Step 6: If a **DVPOBF** interrupt triggers, the host must read the data from the DVPO_FIFO as explained in Section 5.6.2 “Reading Data from the DVP Data Register”. If the data type is either a PAUSE_DRIVE or RESUME_DRIVE request, the appropriate action must be taken as explained in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”. This step is only necessary if data is passed via the CD-DSP interface.
Step 7: The host polls the **STATUS1** register, checking for **PICTYPE** not equal to 00b.
Step 8: Once **PICTYPE** is not 00b, issue an **end_playback** command.
Step 9: Repeat steps 3 through 8 as often as necessary.

6.14 Reverse Playback in DVD

A special mode of operation supported for DVD bitstreams is “reverse playback” in which the **ZR36710** will play back I- & P-pictures in reverse order. Two SDRAMs are required for reverse playback support. The protocol between the host and the **ZR36710** to support this feature is given in the microcode release notes.

6.15 Random access

The random access functionality is achieved by using the **end_playback** host command followed by a **start** host command that will start playback of the new bitstream as described in Section 6.11.1 “Operation States of the ZR36710”.

If the *VidEntry* bit of *BitstreamSelect*[1] set-up parameter is equal to 0, then the device will discard incoming bitstream until the first I-picture header, GOP header or sequence header is found and begin decoding at that point. The host should set *VidEntry* to 0 only if it is certain that the video sequence header (and extensions for MPEG-2) that precedes the first found I-picture has exactly the same parameters as the last sequence parameters decoded by the **ZR36710** (including quantization matrices). If *VidEntry* = 1, the device will discard incoming bitstream until the first sequence header is found and begin decoding at that point.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

For VideoCD streams (*CBSelect*[1] = 00000b), there is more to random access than what is described here. Please see Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams” for more information on handling VideoCD streams. Even for VideoCD streams, there are “special” VideoCD streams that are handled with a different sequence of host operations as explained in Section 14.7 “Also For: Random Access for Special VideoCD Streams”.

6.16 Multiple video sequences

When the **ZR36710** encounters a video sequence end code, it will stop decoding the video and display the last decoded picture before the sequence end code. When another video packet of the same video stream is encountered after the video sequence end code, video decoding restarts using the time stamps and the **SCLK** counter as for the first video sequence in the video stream. The ADP continues to output data (if audio is present in the bitstream). For DVD bitstreams, the sub-picture and HLI continue operation. If closed captions is switched on, the *CaptionWord*[1] is inserted.

Playback resumes in the same mode as it was before reaching the sequence end code. For example, if the **ZR36710** was in one of the special modes (e.g. ***Step***, ***Slow***, etc.), playback will resume in these special modes.

The only host commands allowed after decoding the video sequence end code and before beginning of decoding of the next video sequence are:

- **pause_stream**
- **continue**
- **single_stepping**
- **slow_motion**
- **end_playback**

6.17 Host commands for CD-DA

Host commands for playback of CD-DA discs

When playing back CD-DA discs or bitstreams, only the following host commands are legal:

- **start**
- **end_playback**
- **pause_stream**
- **continue**

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

7. Video Scaling and Panning

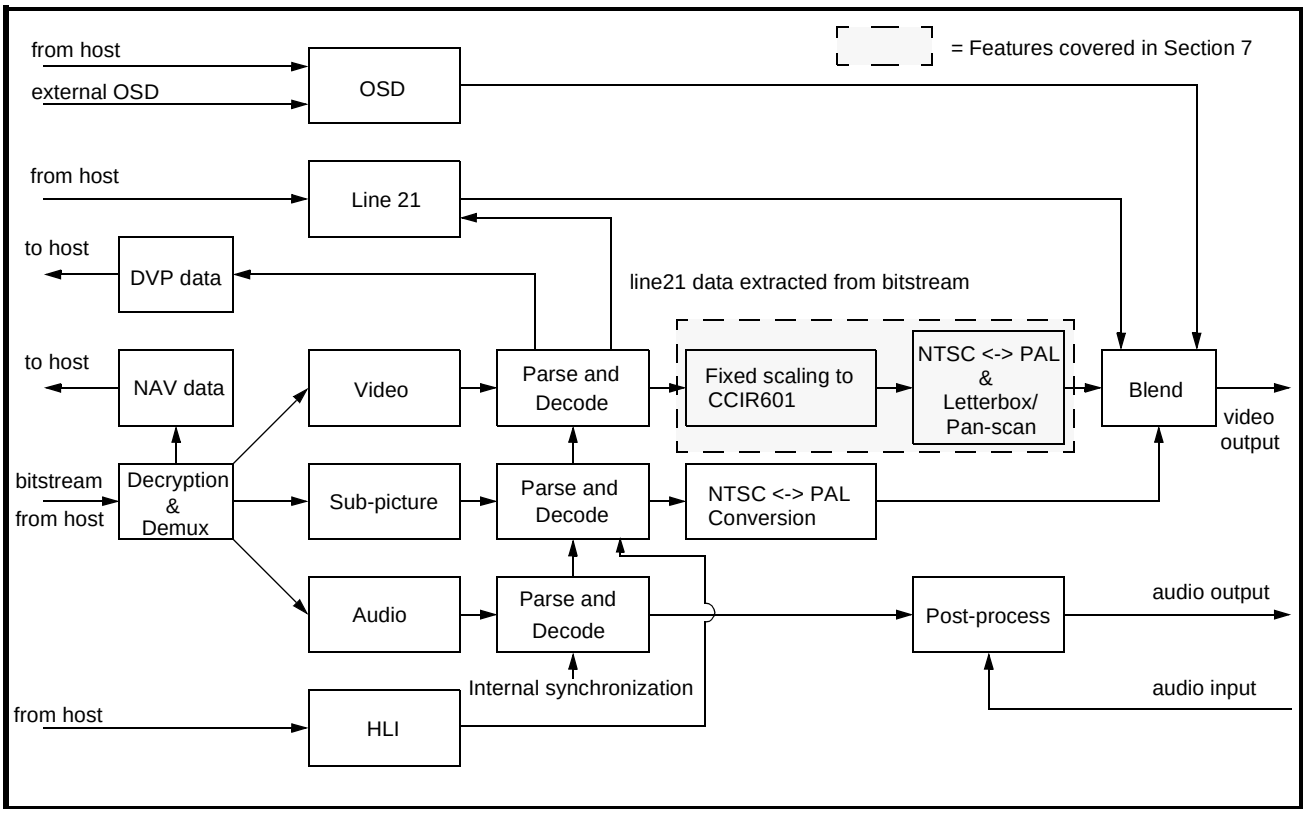

FIGURE 38. Simplified block diagram of **ZR36710** with focus on scaling and panning

To convert a decoded image to an interlaced CCIR size image that has been optionally converted from NTSC <-> PAL (or vice versa), Letterboxed or Pan-scanned (or some other type of display aspect ratio conversion with panning), the **ZR36710** does the following:

- Selects which pixels of the decoded image will be passed to the fixed scaler, performing horizontal and/or vertical panning.
- Performs the necessary fixed scaling to create an interlaced 4:2:2 CCIR-size image.
- Selects which pixels out of the fixed scaler will be passed to the programmable scaler.
- Scales the image, performing pixel aspect ratio conversion for NTSC <-> PAL conversion and display aspect ratio conversion (e.g. Letterbox or Pan-scan).
- Selects the image area size and position on the display.

All of these functions are grouped into two categories: scaling and panning. Each of these categories can be controlled via the host (set-up parameters) or handled automatically by the **ZR36710**. Figure 39 shows the set-up parameters that pertain to these functions when the host is responsible for handling scaling and panning. These parameters are explained in the following sub-sections.

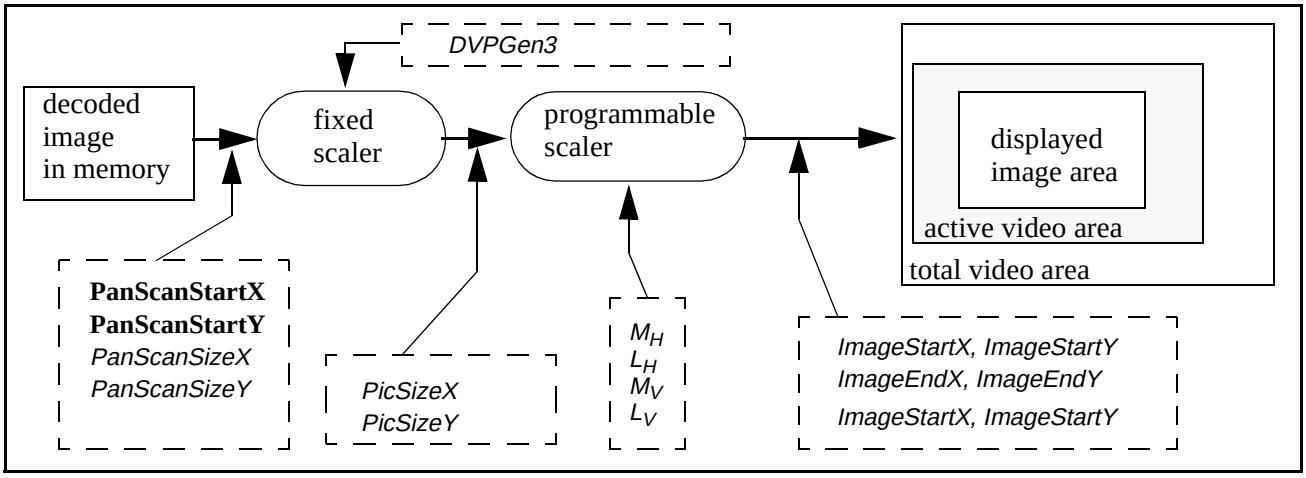

FIGURE 39. Scaling and Panning

7.1 Panning: Which Pixels/Lines to Use in the Decoded Image

If any panning is to be performed (e.g. Pan-scan) on the video, it is handled by selecting which pixels of the decoded image will be used and which pixels will be discarded prior to passing them to the fixed and programmable scalers. The PanScan internal variables and parameters as shown in Table 76 determine which decoded pixels are used for further scaling and which pixels are discarded. The PanScan parameters (see Figure 40) relate to one decoded field (or picture) of the source.

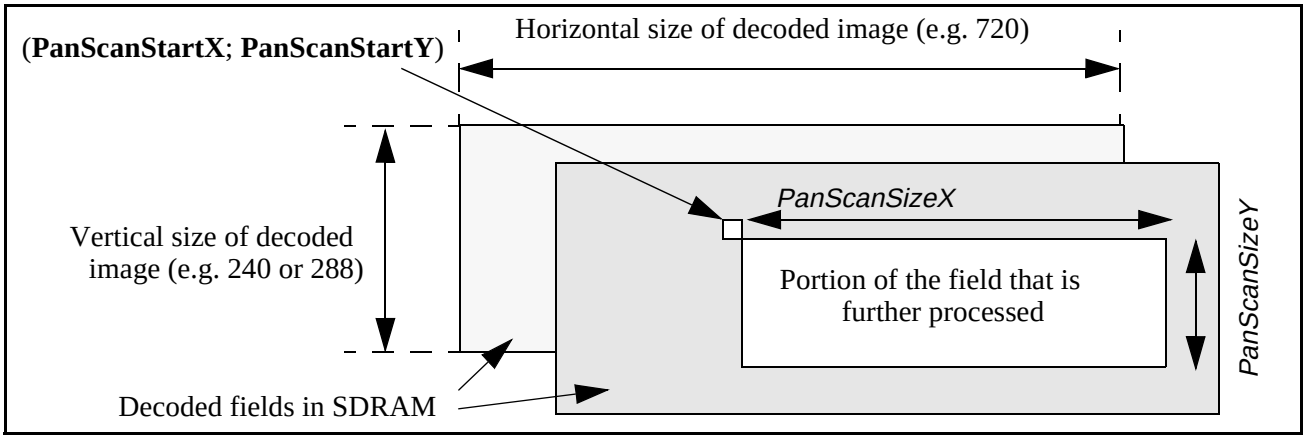

FIGURE 40. PanScan parameters

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TABLE 76. PanScan Parameters

Parameter/Variable	Description	
PanScanBaseX	Used in determining **PanScanStartX** as explained below. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PanScanBaseY	Used in determining **PanScanStartY** as explained below. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PanScanOffsetX	Used in determining **PanScanStartX** as explained below when the host calculates the panning values. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PanScanOffsetY	Used in determining **PanScanStartY** as explained below when the host calculates the panning values. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PanScanStartX	An internal variable calculated within the **ZR36710**, it defines the first pixel per line of the decoded image that is used for further scaling. By setting *AutoPanScan* to 0, the host indicates that it will define **PanScanStartX** completely through set-up parameters. By setting *AutoPanScan* to 1, the host indicates that **PanScanStartX** is adjusted on a frame-by-frame basis by making use of the frame_center_horizontal_offset (FCHO) value extracted from each frame’s picture header.	
	AutoPanScan = 0	**PanScanStartX** = *PanScanBaseX* + *PanScanOffsetX*
	AutoPanScan = 1	**PanScanStartX** = *PanScanBaseX* + FCHO
PanScanStartY	An internal variable calculated within the **ZR36710**, it defines the first line of the decoded image that is used for further scaling. By setting *AutoPanScan* to 0, the host indicates that it will define **PanScanStartY** completely through set-up parameters. By setting *AutoPanScan* to 1, the host indicates that **PanScanStartY** is adjusted on a frame-by-frame basis by making use of the frame_center_vertical_offset (FCVO) value extracted from each frame’s picture header.	
	AutoPanScan = 0	**PanScanStartY** = *PanScanBaseY* + PanScanOffsetY
	AutoPanScan = 1	**PanScanStartY** = *PanScanBaseY* + FCVO
PanScanSizeX	Defines the horizontal size (in pixels) of the portion of the decoded field (or picture) that is further processed. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PanScanSizeY	Defines the vertical size (in lines) of the portion of the decoded field (or picture) that is further processed. Restrictions on this parameter are explained in Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”.	
PicSizeX	Defines the number of pixels out of the fixed scaler that will be passed to the programmable scaler. *PicSizeX* = (r * *PanScanSizeX* - 1), r = 2 if the decoded horizontal size <= 384, otherwise r = 1.	
PicSizeY	Defines the number of pixels out of the fixed scaler that will be passed to the programmable scaler. *PicSizeY* = *PanScanSizeY* - 1.	

Dynamic Panning During Decoding

When *AutoPanScan* = 0, *PanScanOffsetX* and *PanScanOffsetY* can be changed dynamically only during decoding. The change in these values takes effect on the next VSYNC. This allows the host flexibility in its panning options. An alternative method of dynamic panning that includes panning support while decoding is paused is explained in Section 7.7 “Dynamic Panning and Zoom”.

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Phone (408) 919-4111 Fax (408) 919-4122

7.2 Fixed Scaling to CCIR601-Size Interlaced Display Frames

Once the VPU has determined which pixels are to be further processed, the decoded image is presented to a fixed scaler in which frames are automatically scaled to CCIR601 YUV 4:2:2 interlaced resolution (e.g. either 720x240/field for NTSC or 720x288/field for PAL). The fixed scaler performs SIF/Half-D1 size-to-CCIR size conversion by employing horizontal and vertical upscaling as necessary. When appropriate, the **ZR36710** performs field interpolation. The fixed scaler does not perform vertical scaling for NTSC <-> PAL conversion, which is explained further in Section 7.3 “Programmable Scaler”.

Terminology: SIF, Half D1 and CCIR Size

- **VS**: Number of lines in a decoded image as specified by the vertical size value in the sequence header and sequence extension header.
- **HS**: Number of pixels/line in a decoded image as specified by the horizontal size value in the sequence header and sequence extension header.
- **SIF size**: VS <= 288 and HS <= 384.
- **Half D1 size**: VS > 288 and HS <= 384.
- **CCIR size**: VS > 288 and HS > 384.

Supported Sizes of Coded Frames

- **MPEG-2 CCIR size**.
- **MPEG-2 Half D1 size**.
- **MPEG-2 progressive SIF size**. The top field is the horizontally scaled image. The bottom field is vertically interpolated from the top field.
- **MPEG-1 progressive SIF size**. The top field is the horizontally scaled image. The bottom field is vertically interpolated from the top field.
- **MPEG-1 progressive CCIR size** (High Resolution Still Images).

Unsupported sizes

- Interlaced SIF size pictures are not supported.
- Resolutions larger than 720x576 are not supported.

Fixed Scaling for Non-CCIR/Non-SIF/Non-Half D1 MPEG Resolutions, CD-I

Preservation of aspect ratio within the fixed scaler is not guaranteed for images that are not “standard” (e.g. standard is 352x240, 352x288, 720x480, 720x576, 352x480, 352x576).

CD-I (green-book) material with 384 pixels per line is decoded properly, but the host must limit the portion of the decoded image that is further processed (scaled and displayed) to 352 (or less) pixels, using the PanScan parameters as explained in Section 7. “Video Scaling and Panning”. Thus, CD-I material of 384 x 208 (256) is displayed at a maximum resolution of 704 x 416 (512).

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Phone (408) 919-4111 Fax (408) 919-4122

Forcing Progressive or Interlaced Interpolation

The host can force the **ZR36710** to treat the next displayed picture as a progressive or interlaced picture and thus perform the appropriate interpolation. This is done by writing the appropriate value to *DVPGen3*[1] as follows:

TABLE 77. Force Progressive or Interlaced Interpolation with *DVPGen3*

***DVPGen3* (0x05)**			
15 - 2		**1**	**0**
reserved		Force Interlace	Force Progressive
Reserved bits must be 0.			
Force Interlace	0 = Use data from bitstream to determine interpolation method. Must be 0 if Force Progressive = 1. 1 = Force interlaced picture interpolation method.		
Force Progressive	0 = Use data from bitstream to determine interpolation method. Must be 0 if Force Interlace = 1. 1 = Force progressive picture interpolation method.		

This option can be set during the ***Nspb*** and ***Pause*** states. This option is particularly useful for disabling the field interpolation that typically occurs when the is displaying a paused picture as mentioned in Section 6.11.2 “Host Command: pause_stream”. The chosen interpolation scheme does not take effect until after the decoded image has been displayed for one frame time in the interpolation scheme automatically selected by the **ZR36710** based on data in the bitstream (e.g. as if *Force Interlace* = *Force Progressive* = 0).

7.3 Programmable Scaler

The programmable scaler is the unit that performs the processing required for pixel aspect ratio conversion that is used in NTSC <-> PAL conversion and for display aspect ratio conversion that is used in Pan-scan and Letterbox formatting. It consists of a vertical scaler and a horizontal scaler, both having similar architectures. They may operate concurrently. Each one of the scalers can be used for either up- or down-scaling, depending on the scaling ratio selected by the host or selected automatically.

The concept behind both the horizontal and vertical scalers is a ‘polyphase’ two-tap FIR filter. The tap clock of the horizontal filter is ***VCLK*** and the tap clock of the vertical filter is ***HSYNC***. Each filter supports scaling ratios of (M / L). For the horizontal filter, M and L are given by the M_H and L_H bits of the *ScaleRatio*[1] set-up parameter. For the vertical filter, M and L are given by the M_V and L_V bits of the *ScaleRatio* set-up parameter.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

The following holds true for both the horizontal and vertical scalers:

- $0.75 \leq (M / L) < 2$, where $1 <= M <= 11$ and $1 <= L <= 11$.
- $(M / L) > 1$ results in up-scaling.
- $(M / L) < 1$ results in down-scaling.
- $M = 1$ or $L = 1$ results in bypassing the relevant filter (1:1 scaling ratio effect).

All other combinations of M and L (including M = L != 1, M = 0, L = 0, L > 11 or M > 11) are not allowed and might yield unexpected results. If the host provides the M and L values, the host must ensure that the fraction is reduced:

- Wrong: M = 6, L = 4.
- Correct: M = 3, L = 2.

If the *AutoScaling*[1] parameter is set to allow for the **ZR36710** to perform automatic scaling (automatic calculation of the M and L values), then the device does not make use of the values written to the *ScaleRatio* parameter. The host must write 0x0000 to the *ScaleRatio* parameter if automatic scaling is to be used as explained in Section 7.5 “Automatic Scaling and Image Area”.

7.4 Defining the Image Area of the Scaled Image

The “image area” group of set-up parameters (e.g. *ImageStartX*, *ImageSizeY*) define the positioning of the scaled image within the video output. An image (scaled or not) can be placed on a selected portion of the active video area. The image area size is defined equal to the size of the part of the decoded image, selected for display by the PanScan parameters, after scaling. These parameters are illustrated in Figure 29 and explained in detail in Section 4.5.4 “Definition of the Active Area, Image Area and Background Color”. The image area can be provided by the host or calculated automatically by the **ZR36710**.

Some more restrictions apply for *ImageSizeX* and *ImageSizeY*. The host must make sure that these restrictions are complied with:

- *ImageSizeX* must be an integer multiple of M_H.
- *ImageSizeX* / M_H = *(1 + PicSizeX)* / L_H
- *ImageSizeY* must be an integer multiple of M_V.
- *ImageSizeY* / M_V = *(1 + PicSizeY)* / L_V

If the *AutoScaling* parameter is set to allow for the **ZR36710** to perform automatic image area calculation (automatic calculation of the *ImageStartX*, *ImageStartY*, *ImageEndX*, *ImageEndY*, *ImageSizeX* and *ImageSizeY* values), then the device does not make use of the values written to these parameters. The host must write 0x0000 to these parameters if automatic placement of the image area is to be used as explained in Section 7.5 “Automatic Scaling and Image Area”.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

7.5 Automatic Scaling and Image Area

The programmable scaling and image area placement can be handled automatically within the device by configuring the *AutoScaling*[1] set-up parameter. If this parameter is configured to allow for automatic scaling and image area placement, the host does not need to provide the $M_{(H,V)}$, $L_{(H,V)}$, *PanScanSize(X,Y), PicSize(X,Y), ImageStart(X,Y), ImageEnd(X,Y),* and *ImageSize(X,Y)* parameters.

If two clips with different scaling parameters are played consecutively, the change of scaling parameters is synchronized with the display of the first picture in the latter clip so no incorrect scaling is noticed on the last displayed picture of the former clip. This avoids artifacts when switching from 16:9 to 4:3 clips and vice versa. However, if the two clips have different horizontal_size values in their sequence headers, incorrect scaling may be noticed.

TABLE 78. Automatic Scaling via the AutoScaling set-up parameter.

***AutoScaling* (0x50)**			
15	**14 - 3**	**2**	**1, 0**
DynPanEnable	Reserved	VidFAR	VidFAC
Reserved bits must be 0.			
VidFAR	0 = Display frame aspect ratio is 4:3. Must be 0 if VidFAC = 00b. 1 = Display frame aspect ratio is 16:9.		
VidFAC	00b = Display frame aspect ratio conversion (FAC) is handled by host. 01b = **ZR36710** performs automatic display FAC via horizontal scaling (e.g. Pan-scan). 10b = No display FAC, but will still calculate parameters for 1:1 scaling or NTSC/PAL conversion. 11b = **ZR36710** performs automatic display FAC via vertical scaling (e.g. Letterbox).		

For the **ZR36710** to be able to perform automatic aspect ratio conversion, the device must know what the aspect ratio of the decoded image is (applicable only for DVD bitstreams, *CBSelect*[1] = 00010b). Either the host can inform the **ZR36710** what the decoded aspect ratio is or the device can extract this information from the bitstream. This indication is done through bits 2 and 1 of *DVPGen2*[1], but all other bits of this general DVP input parameter must be left as they were. Other bits are used for other purposes (e.g. NV_PCK retrieval method) and should not be changed. These bits have the following functionality:

TABLE 79. Selecting the decoded image aspect ratio via *DVPGen2* bits 2 and 1

***DVPGen2* (0x04)**			
15 - 3	**2**	**1**	**0**
*	Source	DecAR	*
* = Bits used for other functions that must be left as they were.			
Source	0 = Decoded image aspect ratio is extracted from the bitstream. 1 = Decoded image aspect ratio is selected by DecAR bit.		
DecAR	0 = Decoded image aspect ratio is 4:3. Must be 0 if Source = 0. 1 = Decoded image aspect ratio is 16:9.		

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

7.6 Examples of NTSC <-> PAL, Letterbox and Pan-scan

Table 80 shows the settings for different combinations of standards conversion and display aspect ratio conversion. If the host handles the scaling and placement of the video, these values should be used.

TABLE 80. Display Aspect Ratio and/or Standards Conversion for CCIR size interlaced images

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
From standard	pal	pal	pal	pal	pal	pal	pal	pal	pal	pal
From aspect ratio	4:3	4:3	4:3	4:3	4:3	16:9	16:9	16:9	16:9	16:9
To standard	ntsc	ntsc	ntsc	pal	pal	ntsc	ntsc	ntsc	pal	pal
To aspect ratio	4:3	16:9	16:9	16:9	16:9	4:3	4:3	16:9	4:3	4:3
Conversion axis		V	H	V	H	V	H		V	H
PanScanSizeX	720	720	720	720	720	Unsupported by the **ZR36710**	540	720	720	540
PanScanSizeY	288	216	288	216	288		288	288	288	288
ImageSizeX	720	720	540	720	540		720	720	720	720
ImageSizeY	240	240	240	288	288		240	240	240	288
M_H	1	1	3	1	3		4	1	1	4
L_H	1	1	4	1	4		3	1	1	3
M_V	5	10	5	4	1		5	5	3	1
L_V	6	9	6	3	1		6	6	4	1
	11	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
From standard	ntsc	ntsc	ntsc	ntsc	ntsc	ntsc	ntsc	ntsc	ntsc	ntsc
From aspect ratio	4:3	4:3	4:3	4:3	4:3	16:9	16:9	16:9	16:9	16:9
To standard	pal	pal	pal	ntsc	ntsc	pal	pal	pal	ntsc	ntsc
To aspect ratio	4:3	16:9	16:9	16:9	16:9	4:3	4:3	16:9	4:3	4:3
Conversion axis		V	H	V	H	V	H		V	H
PanScanSizeX	720	720	720	720	720	720	540	720	720	540
PanScanSizeY	240	180	240	180	240	240	240	240	240	240
ImageSizeX	720	720	540	720	540	720	720	720	720	720
ImageSizeY	288	288	288	240	240	216	288	288	180	240
M_H	1	1	3	1	3	1	4	1	1	4
L_H	1	1	4	1	4	1	3	1	1	3
M_V	6	8	6	4	1	9	6	6	3	1
L_V	5	5	5	3	1	10	5	5	4	1

From standard	This is the video standard of the decoded image.
From aspect ratio	This is the display aspect ratio of the decoded image.
To standard	This is the video standard of the display device.
To aspect ratio	This is the display aspect ratio of the display device.
Conversion axis	If the display aspect ratio of the decoded image and the display device differ: V = vertical processing (e.g. Letterbox is 16:9 to 4:3). H = horizontal processing (e.g. Pan-scan is 16:9 to 4:3)

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Phone (408) 919-4111 Fax (408) 919-4122

7.7 Dynamic Panning and Zoom

The **ZR36710** supports dynamic panning of an image even while decoding is paused. Although it may look like modification of the *PanScanOffsetX* and *PanScanOffsetY*[1] parameters (*AutoPanScan* = 0) allows this, this will not work because these parameters only adjust the panning while decoding is taking place. If decoding is paused, the changing of these parameters does not affect the display. Therefore, two other set-up parameters, *DynPanX* (set-up parameter 0xE0) and *DynPanY* (0xE1), are used to adjust the panning offsets while decoding is paused. If desired, these parameters can also be used to pan while decoding occurs.

The *DynPanEnable* bit in the *AutoScaling* set-up parameter determines if **PanScanStartX** and **PanScanStartY** are dependent on *DynPanX* and *DynPanY* as shown in Table 81 . *DynPanX* and *DynPanY* are 16.2 unsigned fractions. Once the *DynPanEnable* bit is set it must remain set until the next frame is decoded, at which time it may be cleared.

TABLE 81. Enabling Dynamic Panning

***AutoScaling* (0x50)**			
15	**14 - 3**	**2**	**1, 0**
DynPanEnable	Reserved	VidFAR	VidFAC
Reserved bits must be 0.			
DynPanEnable	0 = **PanScanStartX** and **PanScanStartY** are calculated as shown in Table 76 . 1 = PanScan values are calculated as follows: **PanScanStartX** = *DynPanX* **PanScanStartY** = *DynPanY*		

If the scaling ratios are selected by the host (*VidFAC* = 00b), the host is not limited to M and L values in the *ScaleRatio* set-up parameter that yield 4:3 <-> 16:9 aspect ratio conversions. The host may enter values for M and L that allow for a “zoom” effect. The limitations for M and L as explained in Section 7.3 “Programmable Scaler” apply and allow for up to a 2X zoom. Since the host must calculate the M and L values, the host may also need to calculate any aspect ratio conversion along with the zoom factors, thus further limiting the effective zoom capabilities.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

8. Closed Captions (“Line 21”) Modulation

Per federal regulations, all TV sets sold in the U.S. (NTSC) have the ability to decode and display closed caption data modulated on the 21st video line. The **ZR36710** supports modulation of closed caption data on a selected line (programmable).

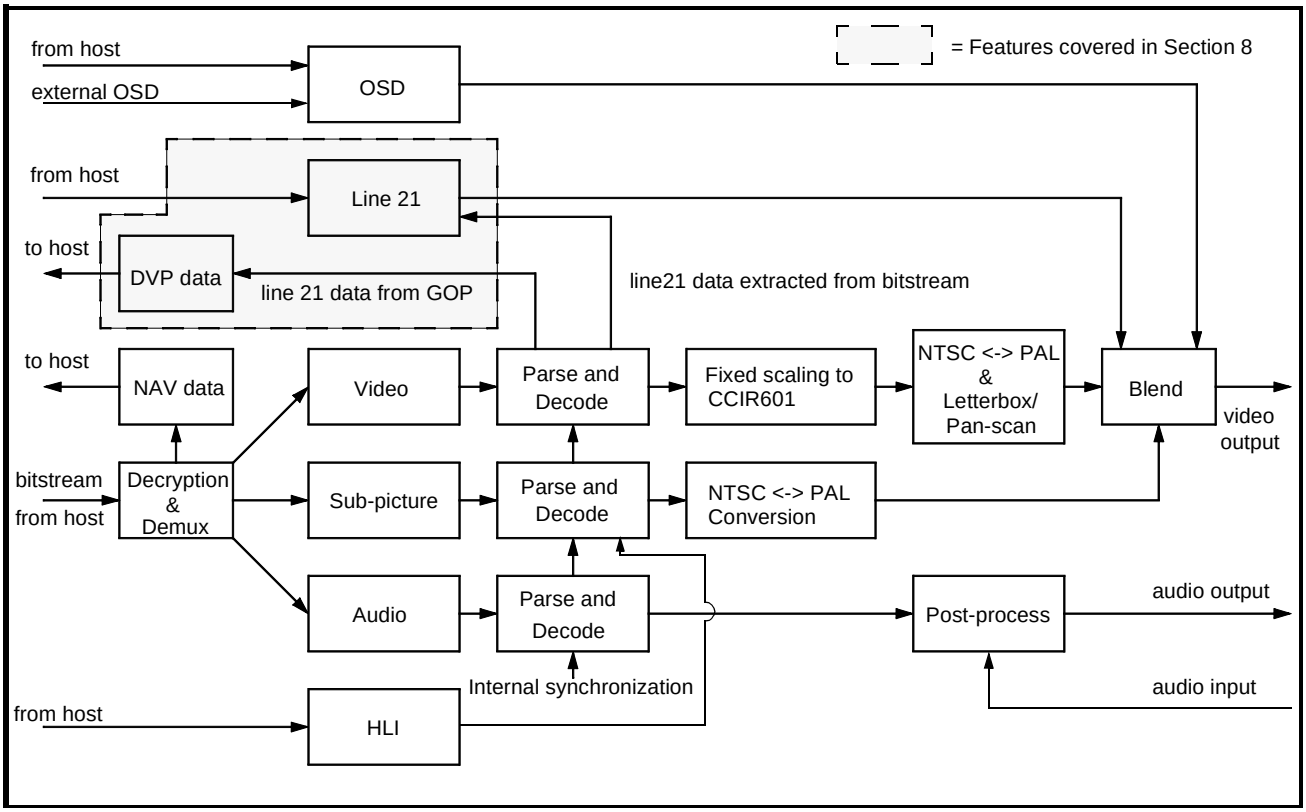

FIGURE 41. Simplified block diagram of the **ZR36710** with focus on the closed-captions processor

The DVD specification supports inclusion of closed captions data as a special type of MPEG-2 or MPEG-1 user_data in the GOP layer. The **ZR36710** extracts this data and modulates it on a host-selected (e.g. 21st) video line in compliance with the EIA-608 standard. The block within the device that performs this modulation is referred to as the “Closed Caption Modulator”, or CCM. This data is also provided to the DVPO_FIFO as explained in Section 5.6.2 “Reading Data from the DVP Data Register”, making the closed caption data available to the host.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

8.1 Control Over Closed Captions Modulation

Closed captions modulation is enabled or disabled through the *CaptionSwitch*[1] parameter. If it is disabled (*CaptionSwitch* = 0x0000), then no modulation will be done, even if line 21 data appears in the bitstream.

Normal operation of the CCM occurs when *CaptionSwitch* = 0x0002. For special modes of operation, such as pausing playback, PAL to NTSC frame rate conversion, or other situations in which closed caption data is not contained within the bitstream, the **ZR36710** automatically inserts a pair of characters on the closed caption line. This pair of characters is provided by the host as a 16-bit parameter called *CaptionWord*[1]. The host should initialize *CaptionWord* to 0x0000 (the NOP command, as explained in Section 8.3 "Line 21 in PAL and in NTSC/PAL Conversion") prior to any playback.

A debugging mode is engaged by setting *CaptionSwitch* = 0x0001. In this case the **ZR36710** will repeatedly modulate one pair of characters (*CaptionWord*) on every field, regardless of the line 21 information that appears in the bitstream.

Following is a description of the CCM behavior in several different circumstances:

- When the CCM is disabled (*CaptionSwitch* = 0x0000), it does not modulate anything; It outputs background.
- When the CCM is enabled (*CaptionSwitch* = 0x0002), its output depends on the host command recently issued as explained in Section 6.11 "Host Commands and Control over the Playback Operation".
- If a change is made to the video stream ID, the CCM will repeatedly modulate the *CaptionWord* until the new Line 21 GOP is loaded to the CCM_FIFO.
- Line 21 'starving': whenever the CCM has to modulate line 21 data, but for some reason the CCM_FIFO is empty, the CCM will modulate the *CaptionWord* until data is available in the CCM_FIFO.

Regardless of the value in the *CaptionSwitch* parameter, the GOP data will always be copied to the DVPO_FIFO and made available to the host.

8.2 Actual 'Line 21' Positioning

The **ZR36710** matches the closed captions vertical coordinates to its video front-end, using the 5-bit *CaptionOffset*[1] parameter provided by the host. *CaptionOffset* ranges from 0 to 31 lines. Thus, in practice, the line 21 data will be modulated over the video line number indicated by *CaptionOffset*.

For proper closed captions modulation, *ActiveSizeX*[1] must be set to 720.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

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8.3 Line 21 in PAL and in NTSC/PAL Conversion

According to the DVD Specifications 1.0, PAL sources are not supposed to include line 21 information. However, in case such sources are encountered, and the closed captions information is presented in a similar way to that in NTSC (i.e. through GOP user_data), the **ZR36710** will modulate this information.

NTSC to PAL

In case of 29.97 fps to 25 fps conversion, the **ZR36710** does not modulate closed captions information.

PAL to NTSC

In case of 25 fps to 29.97 fps conversion, the CCM inserts one dummy closed captions information field after every 5 “real” closed captions fields. The two characters that are inserted in the dummy added field are provided by the host as a 16-bit parameter, *CaptionWord*. It is intended that the host will insert a pair of characters that are interpreted by the closed captions decoder as a “no change” instruction, or NOP (0x0000).

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Phone (408) 919-4111 Fax (408) 919-4122

9. On-Screen Display

The on-screen display (OSD) overlay processor of the **ZR36710** allows the host to upload complete lines of OSD into a buffer in the device's SDRAM through the host bus, select the pixel colors and display selected lines of OSD anywhere on the active portion of the display. Blending factors for each color can be selected, allowing blending of the OSD with the video content. Lines of OSD can be configured to "blink" on and off approximately every half-second. The OSD buffer in SDRAM can be configured as either one or two planes, allowing different OSD displays for each field of video, and the **ZR36710** can automatically switch between the two planes on a field-by-field basis or just display one of the planes on both fields. Two color palettes are allocated and selected on a line-by-line basis. Each line of OSD can make use of either color palette, no matter within which plane the line is placed. An external OSD interface allows for real-time placement of OSD data onto the video content.

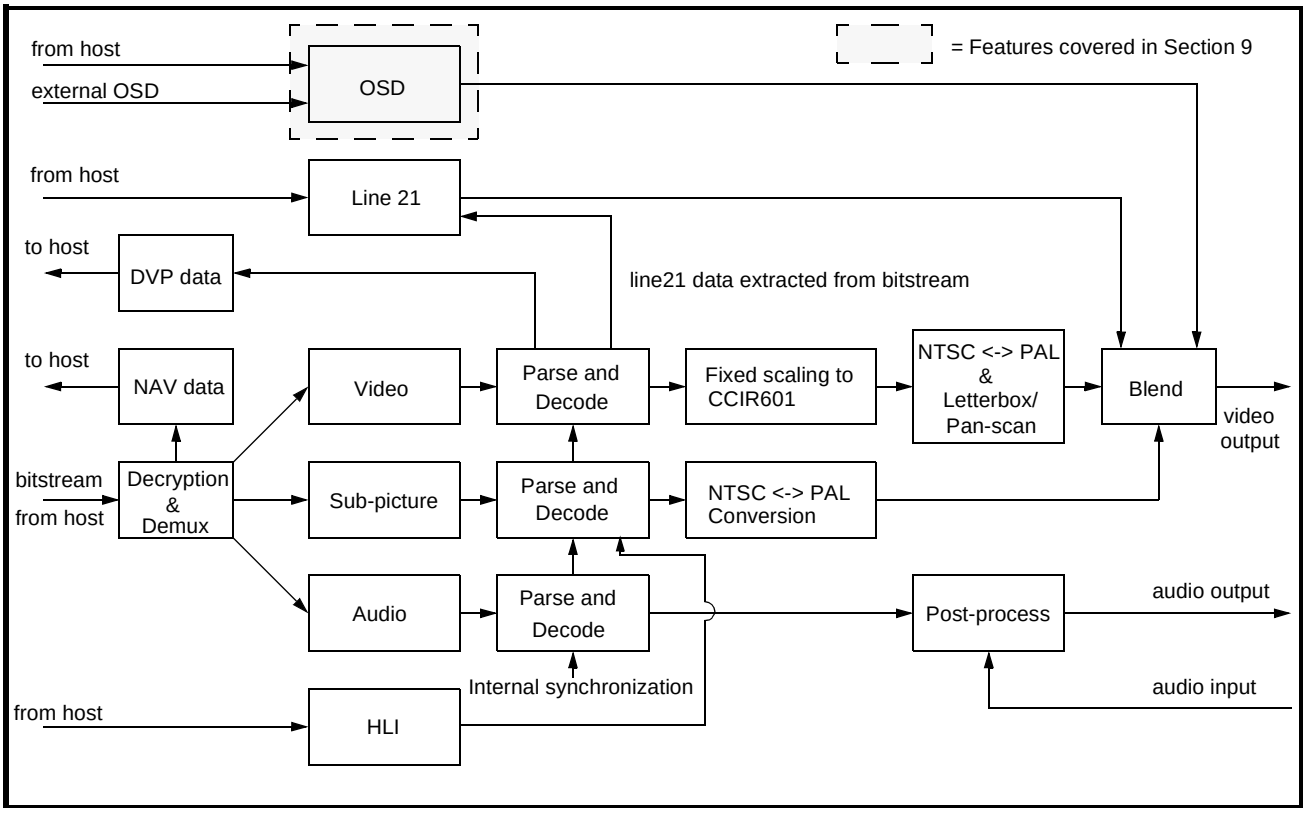

FIGURE 42. Simplified block diagram of the **ZR36710** with focus on OSD.

When enabled, OSD does not depend on the decoding state of the device. OSD may be active whether or not the **ZR36710** is decoding.

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Phone (408) 919-4111 Fax (408) 919-4122

9.1 OSD Buffer in SDRAM

An OSD buffer is constantly allocated in SDRAM for OSD data. The default size of the OSD buffer is 52KBytes, but once microcode is loaded to the device, the microcode determines the size of the OSD buffer. The maximum size of this buffer is determined by the number of planes it is configured as (explained in the following sub-section), either 128 KBytes for a single plane or 256 KBytes as two planes. If configured as a single plane, the size of the buffer must be a multiple of 1 KByte. If configured as two planes, the size of the buffer must be a multiple of 2 KBytes.

The data is represented in the SDRAM buffer as lines of pixels. Each line contains header information that indicates how many active lines should be skipped after displaying the associated OSD line before displaying the next OSD line in the buffer. This method saves space in the buffer by not having to write lines of transparent OSD that correspond to the active lines where no OSD should appear.

9.1.1 Single or Dual-Plane Structure

The OSD buffer can be configured in two ways through the *OSDMem* bit of the *OSDControl*[1] set-up parameter. To illustrate these points, an example is given in which the complete OSD buffer size is 52x1024 bytes:

- A single plane of the complete buffer size, e.g. 52x1024 bytes (*OSDMem* = 0).
- Two switchable planes (denoted plane 0 and plane 1) of equal size, e.g. 26 x 1024 bytes each (*OSDMem* = 1). In this example, the first plane, denoted plane 0, is mapped to the first 26 x 1024 bytes of the OSD memory, and the second plane, denoted plane 1, is mapped to the next 26 x 1024 bytes of the OSD memory.

When the dual-plane structure is selected, the OSD decoder displays data from one plane, while data can be loaded to the second plane (‘off-screen’ plane). There are several methods of switching between the planes, determined by *OSDSwitchPlane* bits of the *OSDControl* set-up parameter:

- *OSDSwitchPlane* = 00b, The planes are toggled every effective edge of ***VSYNC***. Plane 0 is always associated with the top field, and plane 1 with the bottom field. If *OSDMem* = 0, then these bits must also be 00b.
- *OSDSwitchPlane* = 01b, The planes are toggled every effective edge of ***VSYNC*** at the beginning of the top field (every display frame).
- *OSDSwitchPlane* = 10b, A switch to plane 0 is done on the next effective edge of ***VSYNC***. No further toggling takes place.
- *OSDSwitchPlane* = 11b, A switch to plane 1 is done on the next effective edge of ***VSYNC***. No further toggling takes place.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

9.1.2 OSD Line Structure in SDRAM

Each line of OSD data is not just a simple bitmap, but rather must be formatted to a "line structure" compatible for the **ZR36710**. Every display line in the SDRAM buffer is represented by a line header and the pixel data of this line. Figure 43 depicts the structure of an OSD line.

The line header contains the 'hole size', described as a number of field lines (ranging from 0 to 239 (NTSC) or 287 (PAL)) which has no OSD data, and three display control information bits for this line: Blinking, Transparency, and Palette number as explained below.

OSD Line Header Structure

- **hole size** indicates the number of display lines that should be skipped after displaying the line to which the header belongs and before displaying the next OSD line. A hole size of 0 means no hole; The next OSD line should be displayed on the next display (field) line. The purpose of supporting 'holes' is to let the host insert transparent lines without wasting any OSD buffer space.
- **Palette number** indicates which of the two OSD palettes (0 or 1) should be used with this line.
- **Transparency** indicates if the line is (completely) transparent or not. If it is not transparent, the blending information of every pixel is determined by the pixel value itself (by the corresponding *OSDBF*[1] value in the palette). Although transparent lines can simply be omitted from the OSD buffer, it may be worthwhile for the host to upload transparent lines only if their transparency status has to be changed later.
- **Blinking** indicates if this line blinks. All blinking lines toggle (together) between a state of visible and non-visible every 16 display frames.

OSD Pixel Data Structure

Following the line header, the OSD line contains pixel data accounting for every pixel in the active video area. The pixel data of every line describes the *ActiveSizeX*[1] pixels (up to 720 pixels) of the line in one of two methods, selected by the *OSDDot* bit of the *OSDControl*[1] set-up parameter:

- *OSDDot* = 0, 4 bits are used for each pixel.
- *OSDDot* = 1, 4 bits are used for each pair of pixels (pixels 0 and 1 are a pair, 2 and 3,..., 718 and 719).

OSDDot is applicable for both OSD planes (if *OSDMem* = 1). The 4-bit pixel values reference an OSD palette value as explained in the following section.

If *OSDDot* = 0 and the OSD data is blended with the source material via the *OSDBF* value (either 01b or 10b) as explained in Section 9.2 "OSD Pixels and Palette", then for each pair of pixels (pixels 0 and 1 are a pair, 2 and 3, ..., 718 and 719) only the Y component is allowed to change; The U, V and *OSDBF* values must remain the same for each pair. For example, if pixel 4 has U = 28, V = 76 and *OSDBF* = 01b, then pixel 5 must have U = 28, V = 76 and *OSDBF* = 01b as well.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

The host is responsible to make sure that the number of OSD pixels following every line header matches the *OSDDot* parameter and the *ActiveSizeX* parameter. The following equation must be fulfilled:

- Number of OSD pixel-data bytes in OSD line = *ActiveSizeX* * [0.5 / (*OSDDot* + 1)]

Note that *ActiveSizeX* is an integer multiple of 8, so the line size (including the header) is always an even number of bytes.

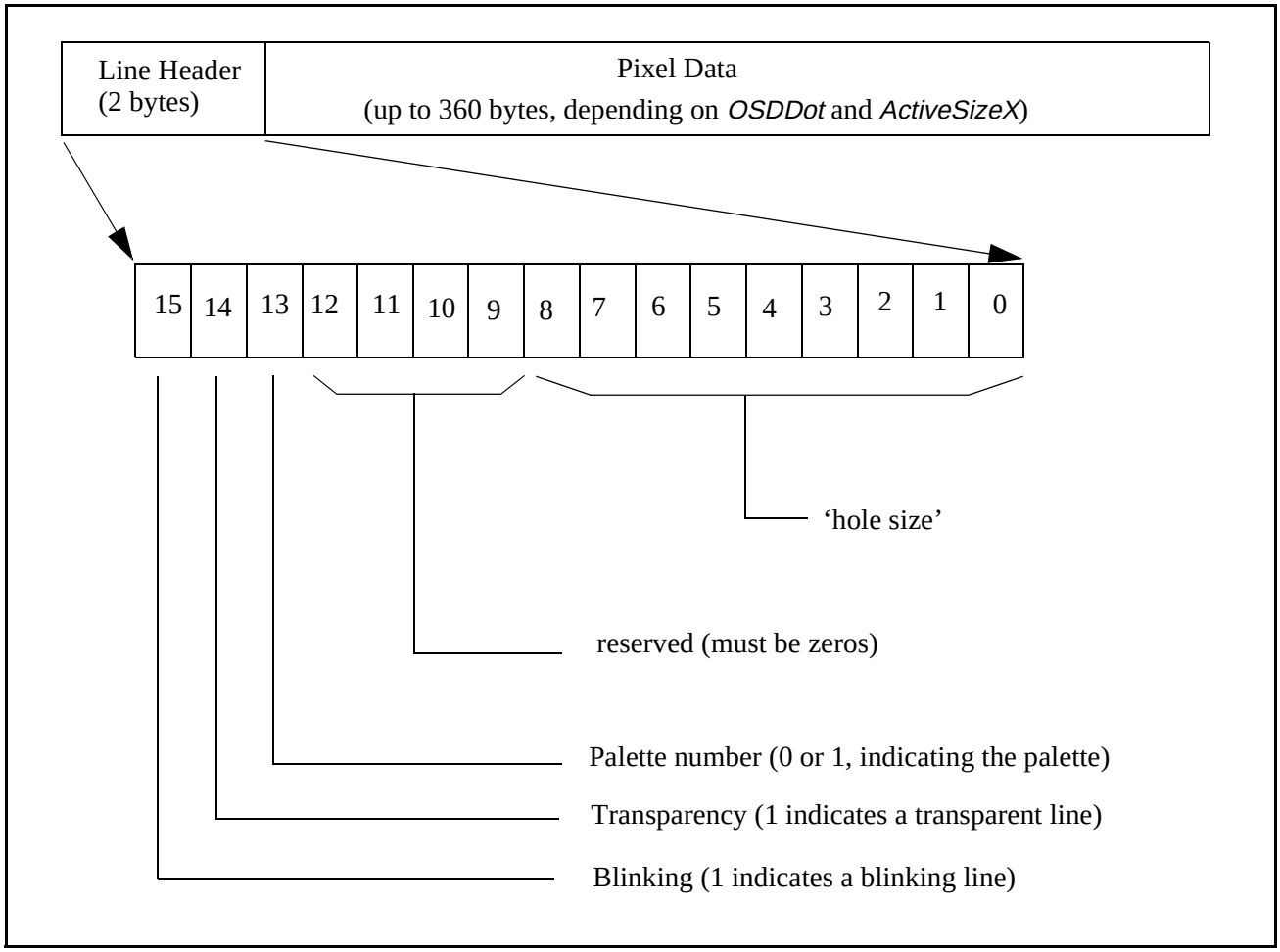

FIGURE 43. OSD line structure

Number of Lines Supported in the OSD Buffer

A plane in the OSD buffer, whether the buffer is one plane or two, is associated with a single field. Unless *OSDMem* = 1 and *OSDSwitchPlane* = 00b, the OSD data from a plane is duplicated for both fields.

Full OSD display frame resolution is achieved by setting *OSDDot* = 0 (4-bits/pixel), setting *OSDMem* = 1 (two planes), loading appropriate pixel data to each of the planes, and setting *OSDSwitchPlane* = 00b (toggle OSD planes on a field-by-field basis). The number of OSD lines that can be defined with 4 bits per pixel is limited by the size of the OSD buffer size in SDRAM. For example, if a 52KB OSD buffer is allocated, the maximum number of OSD lines supported is 192/display frame or 96/field.

9.2 OSD Pixels and Palette

OSD pixels consist of four bits. The **ZR36710** uses the 4-bit pixel value as an entry to a 16-value palette. Each value in the palette consists of 32 bits, *P[31:0]*, interpreted as follows:

P[31:26] - not used, must be 0x00.

P[25:24] - blending factor, denoted *OSDBF*.

P[23:16] - Y value

P[15:8] - U value

P[7:0] - V value.

- *OSDBF* = 00b, only the content data pixel (video, sub-picture, background) is visible.
- *OSDBF* = 01b, the blending ratio is 1/4 OSD and 3 /4 content data pixel.
- *OSDBF* = 10b, the blending ratio is 1/2 OSD and 1/2 content data pixel.
- *OSDBF* = 11b, only the OSD pixel is visible.

Note if the Transparency bit in the line header for the line is 1, it overrides *OSDBF*.

The **ZR36710** keeps two OSD palettes, *OSDPalette0* and *OSDPalette1*[1]. They are mapped as 2 x 16 parameters (of 4 bytes each) in the set-up parameter space of the **ZR36710**.

The Palette number value of each OSD line header determines which palette is used for the associated line. A palette can be updated anytime, but for proper operation it should be updated only when it is not being used by any lines in the active OSD plane or if OSD is disabled. Otherwise, temporary artifacts may appear onscreen if a palette is changed while in use.

9.3 Uploading OSD Lines - The OSD Address and Data Registers

Uploading of OSD data is done by first writing the required OSD address to the OSD Address Register, than writing the OSD data to the OSD Data Register. The OSD address is a relative (word) address. In the example used in this section in which the OSD buffer is 52KB, address 0x0000 points to the beginning of plane 0, address 0x33FF to the last word (16 bits) of this plane, address 0x3400 points to the beginning of plane 1, and address 0x67FF to the last word of plane 1. In case that the OSD buffer is

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

configured as a single plane, the range 0x0000 to 0x67FF constitutes the plane. Addresses beyond this range are not allowed. Odd addresses are not allowed. The number of bytes written to the OSD Data Register must be even.

The host must not exceed the OSD buffer allocation by starting with an address that is N words before the end of the 52KByte region and then writing more than N words.

The detailed protocol for accessing the OSD buffer is described in Section 5.11 “Writing OSD Data - Reg. 0xB and 0xC (Write)”.

Loading data to an OSD plane that is currently active might result in unexpected temporary visible effects. It is the responsibility of the host to load data to the ‘off-screen’ plane, or to an area in the ‘on-screen’ OSD buffer that is known not to be currently displayed to avoid temporary artifacts.

9.4 Selecting and Placing OSD Lines on the Display

The host must define the portion of each OSD plane (or the one plane, in single plane mode) that is displayed. This is done by two set-up parameters:

- *OSDMemStart*[1] defines the starting (byte) address (relative to the start of the OSD plane in SDRAM) of the first header byte of the first OSD line to display.
- *OSDMemSize*[1] defines the size (in bytes) of the memory portion actually used for OSD, relative to *OSDMemStart*.

Since the OSD generator block treats the OSD area in SDRAM is a cyclic buffer, it may be possible that the sum of *OSDMemStart* and *OSDMemSize* will be larger than the size of the buffer (if the single plane mode is used). After every effective edge of ***VSYNC,*** the **ZR36710** will display only the portion of the OSD memory that is defined valid by *OSDMemStart* and *OSDMemSize*.

9.4.1 Positioning OSD on the Display

Two set-up parameters, *OSDFirstLine* and *OSDLastLine*[1], determine the display field line numbers where OSD is shown. These parameters allow the displayed position of an OSD line in the OSD memory to be changed (vertically) by just modifying these two parameters. These parameters can be changed at any time and the new values become effective on the next effective edge of ***VSYNC***.

- *OSDFirstLine* is the number of lines after the line indicated by *ActiveStartY*[1] before the first OSD line is displayed. The first video line number per field that OSD is displayed is defined by *ActiveStartY* + *OSDFirstLine*.
- *OSDLastLine* is the number of lines after the line indicated by *ActiveStartY* before the last OSD line is displayed. The last video line number per field that OSD is displayed is defined by *ActiveStartY* + *OSDLastLine*.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

The first line defined by *OSDMemStart* and *OSDMemSize* is positioned by *OSDFirstLine*. The number of lines (including skipped lines) to display as defined by *OSDMemSize* should match the number of lines to display as defined by *OSDLastLine - OSDFirstLine.* If there is no match, the smaller of the two will be over-laid, starting with *OSDFirstLine* and *OSDMemStart*.

9.4.2 OSD Vertical Scrolling

By proper usage of the *OSDFirstLine*, *OSDLastLine*, *OSDMemStart*, and *OSDMemSize* parameters, the host can achieve a scrolling effect with negligible overhead and no need to rewrite to the OSD memory. For example, the host may define a certain OSD display window, using *OSDFirstLine* and *OSDLastLine*. It can then direct a certain selected portion of OSD memory onto this display window, using *OSDMemStart* and *OSDMemSize*. By incrementing *OSDMemStart,* but leaving *OSDMemSize, OSDFirstLine* and *OSDLastLine* constant, a scroll-up effect is achieved. This includes the case that OSD information, stored in the upper portion of the OSD memory, can appear below OSD information that appears in the bottom portion of the OSD memory. A scroll-down effect is achieved by decrementing *OSDMemStart* while leaving *OSDMemSize, OSDFirstLine* and *OSDLastLine* constant.

9.5 Blending OSD with Source Material

Prior to blending the OSD with the content (or background), it is re-formatted from the 4:4:4 (24-bit/ pixel) format resulted from the palette, to 4:2:2 (16-bit/pixel) format.

If *OSDDot* = 1 every OSD 4-bit pixel value corresponds to two neighboring video display pixels. In this case, the Y value is duplicated for the two pixels and the U and V values are associated with the two video display pixels as “normal” YUV 4:2:2 format.

If *OSDDot* = 0 every OSD pixel in an even location in line (0, 2, 4, ...) is taken as a 24-bit value (Y, U, V) and from every OSD pixel in an odd location in line (1, 3, ...) only the Y value is taken (The U, V values of its predecessor are associated with it).

Next, the OSD pixel is blended with the content pixel according to the description in 9.2 “OSD Pixels and Palette”.

9.6 Extended OSD Functionality - Full-Screen Support

The previous sections have explained the “normal” operation of the OSD processor, but this operation does not allow for full-screen, 720x576, 4-bits per pixel OSD resolutions. To allow for this support, the host must excute a slightly different protocol to what is explained in earlier sections. Changes/ requirements:

- Two SDRAMs are required. One SDRAM cannot have a large enough OSD buffer allocated for full-screen support.
- Special microcode that allocates the full-screen OSD buffer is required.
- Reserved Write Registers 0xE and 0xF are used to write the OSD data to the OSD buffer as shown in Table 82 . Writing to OSD Address and Data registers 0xB and 0xC as explained in Section 5.11 “Writing OSD Data - Reg. 0xB and 0xC (Write)” does not allow access to the full range of addresses required for full-screen support.

TABLE 82. Extended Protocol of Writing Data to the OSD Buffer for Full-screen Support

Extended Protocol
Step 1: The host writes a base address (each address points to a word, not a byte) to Register 0xE, indicating the starting address within the SDRAM that OSD words will be written to. This address is 32-bits and the full 32-bit address must be written to this register (m.s. word/byte first). The microcode release notes will identify the starting address within the SDRAM that the OSD buffer begins (i.e. the address that the host must write). A write to this address register immediately sets **DRAMBE** = 1 in the **STATUS0** register.
Step 2: The host writes up to 32 words of OSD data to Register 0xF. These words are loaded into a 32-word FIFO. As soon as there is data in this FIFO, **DRAMBE** switches to 0.
Step 3: Once the 32nd word is written to Register 0xF, the **ZR36710** retrieves the data from the FIFO and copies it into the OSD buffer in SDRAM. Once all 32 words are retrieved from the FIFO, the **DRAMBE** bit is set to 1.
Step 4: The host checks for **DRAMBE**[a] = 1 if the host will transfer more data.
Step 5: Once **DRAMBE** = 1, the host may write up to 32 words to Register 0xF. The **ZR36710** will automatically increment the address pointer within the buffer so the host is not required to load a new address to Register 0xE.
Step 6: This process of checking for **DRAMBE** = 1 and writing 32 words to Register 0xF (steps 4 and 5) is repeated as frequently as necessary, depending on how much data must be written into the OSD buffer.
Step 7: If less than 32 words are written to Register 0xF, the host must write 0xFFFFFFFF to Register 0xE to indicate that there are less than 32 words in the FIFO and thus the **ZR36710** will read these words. Without writing 0xFFFFFFFF to Register 0xE, the **ZR36710** would have no indication to read the words in the FIFO.
Step 8: Once the host is finished writing data to Register 0xF (whether or not a complete 32 words were written to the FIFO), the host writes 0xFFFFFFFF to Register 0xE.

a. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

- The *OSDMemStart* and *OSDMemSize* set-up parameters are increased from 16 bits to 21 bits to accomodate the larger OSD buffer. Bits 15 - 0 for each of these parameters is still written to the original set-up parameters, but bits 20 - 16 are written to reserved set-up parameters 0x26 and 0x27 as shown in Table 83 .

TABLE 83. Expanding *OSDMemStart* and *OSDMemSize* for Full-Screen OSD Support

***OSDMemStart Extension* (0x26) and *OSDMemSize Extension* (0x27)**	
15 - 5	**4 - 0**
reserved	Bits 20 - 16
Reserved bits must be 0.	
Bits 20 - 16	These 5 bits expand the *OSDMemStart* and *OSDMemSize* parameter to 21 bits.

9.7 Using an External OSD Device

A control bit in the *VidConfig*[1] parameter can instruct the **ZR36710** to suspend the on-chip OSD engine and instead use an external OSD device. This is possible only when the **ZR36710** outputs the video in 8-bit format (*Video8*[1] = 1). In this case the OSD palettes (same palettes described earlier in this chapter) are used with external signals instead of pixel values from memory.

In this case the ***C[4:0]*** pins are defined as the following input signals:

- ***C[4]*** = ***OSDPLT***: A low level on this input indicates using *OSDPalette0*, a high level indicates using *OSDPalette1*. As shown in Figure 48, there is a 3 pixel delay when the change in palette takes effect.
- ***C[3:0]*** = ***OSDPEL[3:0]***: This is the OSD pixel value. These four signals form a 4-bit entry into the designated OSD palette. ***OSDPEL[3]*** (***C[3]***) is the m.s. bit, ***OSDPEL[0]*** is the l.s. bit.

These signals are sampled on the rising edge of ***VCLKx2*** qualified by (***VCLK*** != *VCLKPol*[1]). These values take effect with the fourth next rising edge qualified by (***VCLK*** != *VCLKPol*). Refer to Section 11.4.1 " Video Interface Timing" for exact timing information.

OSDPEL[3:0], after being converted in the palette, is a 24-bit pixel (plus 2-bit blending factor). The YUV 4:4:4 to YUV 4:2:2 re-formatting is done as follows:

- Every OSD pixel in an even location in line (0, 2, 4, ...) is taken as a 24-bit value (Y, U, V) and from every OSD pixel in an odd location in line (1, 3, ...) only the Y value is taken (The U, V values of its predecessor are associated with it).
- The *OSDBF* value for each pair of pixels must be the same.

The external OSD data is overlaid only within the boundaries of the active video area of the **ZR36710**. Outside of the active area boundaries, the **ZR36710** outputs the background color regardless of the value on ***OSDPEL[3:0]***.

The parameters of the internal OSD engine (*OSDMem*, *OSDMemStart*, *OSDMemSize*, *OSDSwitchPlane*, *OSDDot*, *OSDFirstLine*, *OSDLastLine*) are ignored by the **ZR36710** when the external OSD is chosen.

Typical External OSD Application

Typically, an external OSD device would use only the ***VCLK*** (13.5 MHz), ***VSYNC*** and ***HSYNC*** outputs of the **ZR36710**. It would output three RGB output lines, one on/off output line, and in some cases, a background/foreground output line.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

The R,G,B and on/off lines will be grouped together as ***OSDPEL[3:0]*** inputs of the **ZR36710**. With adequate palette values loaded to the **ZR36710**, the original meaning of these lines can be restored.

The background/foreground output would typically be used to switch between two intensity levels of OSD. This effect can be achieved if this line is connected to the ***OSDPLT*** input, provided that the two palettes are all the same but different intensity levels (Y values).

Note that in such a typical case the ***OSDPEL[3:0]*** value is changed following every (rising edge of) ***VCLK*** (not ***VCLKx2***).

10. Video Blending

The last step of the video processing unit (VPU) is to blend the video, background, sub-picture with HLI, closed captions, and OSD prior to outputting the pixel data.

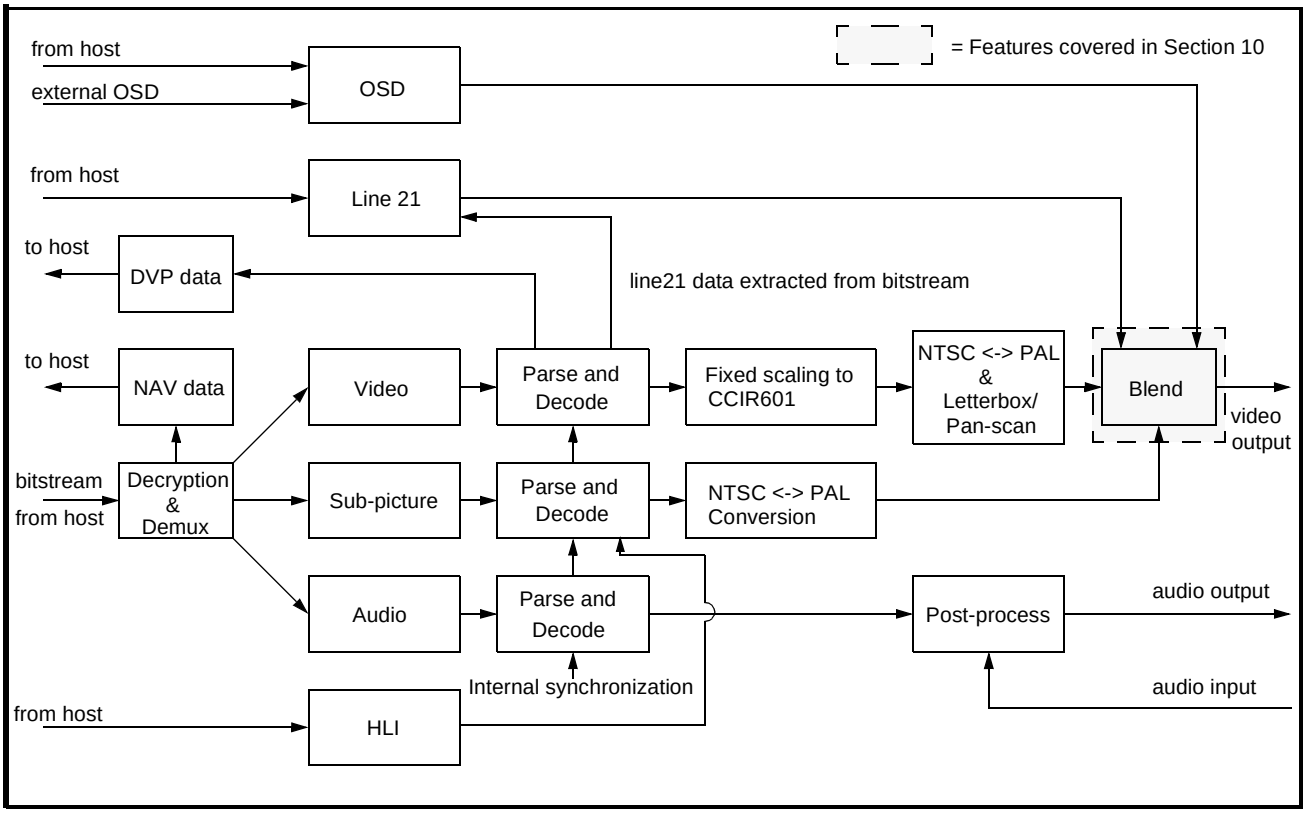

FIGURE 44. Simplified block diagram of the **ZR36710** with focus on blending.

Background Color

The background color is used to "wrap" the MPEG image in cases where it is smaller than the active video window (which is typically 720 by 480 (NTSC) or 576 (PAL)). The background color is set through the *ColorY*, *ColorU* and *ColorV*[1] 8-bit parameters or is forced to black by the *Black* bit of the *PlaybackMode*[1] parameter while a decoded image is displayed. During decoding, the area of background display is the active area excluding the area of the decoded, scaled image. When decoding is not done, the selected background color may be shown on the full screen, depending on various parameters and host commands.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

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Phone (408) 919-4111 Fax (408) 919-4122

Blending MPEG with Sub-picture

In cases of DVD sources, the decoded image may have to be blended with sub-picture data provided by the sub-picture decoder.

In cases were sub-picture pixels exist in pixel locations where MPEG pixels do not exist, the sub-picture is blended with the background color selected at that time. Refer to Section 6.8 “Sub-Picture Decoding with HLI Support” for further information on sub-picture blending with content.

Blending MPEG, Sub-picture and Background With OSD

The blending of OSD pixels with content data is described in Section 9.5 “Blending OSD with Source Material”.

Closed Captions Insertion

Line 21 data is inserted on a line within the vertical blanking region as specified by the *CaptionOffset*[1] set-up parameter. Line 21 data consists only of black and white pixels for proper closed captions support. See Section 8. “Closed Captions (“Line 21”) Modulation” for further details on Line 21 insertion into the video.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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11. DC and AC Characteristics

11.1 ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-65°C to +150°C

Supply Voltage to Ground ..... -0.5V to +5.5V

DC Voltage Applied to Outputs for High Impedance Output State..... -0.5V to +5.5V

DC Input Voltage..... -0.5V to +5.5V

DC Output Current, into Output .....20mA/output (total 200 mA)

DC Input Current..... -10mA to +3.0mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

11.2 OPERATING RANGE

Temperature.....$0°C < T_A < +70°C$

Supply Voltage.....$3.15V < V_{CC} < 3.45V$

October, 1998

11.3 DC CHARACTERISTICS

TABLE 84. DC Characteristics

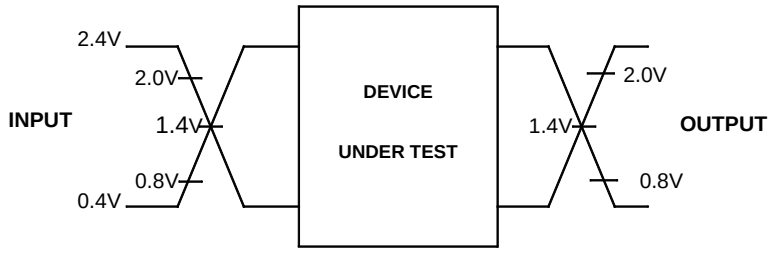
Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	5.5	V	
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = 0.4 mA
$I_{CC\ (3.45v)}$	Power Supply Current	–	360	mA	f = 81 MHz, V_{CC} = 3.45V
$I_{CC\ (3.3v)}$	Power Supply Current	–	330	mA	f = 81 MHz, V_{CC} = 3.3V
I_{stby}	Stand-by Current	–	35	mA	f = 81 MHz, V_{CC} = 3.45V
I_{LI}	Input Leakage Current (1)	--	$\pm$10	uA	See note 1
I_{LO}	Output Leakage Current (1)	--	$\pm$10	uA	See note 1
I_{LI}	Input Leakage Current (2)	--	100	uA	See note 2
I_{LO}	Output Leakage Current (2)	--	100	uA	See note 2
C_{IN}	Input Capacitance	–	10	pF	
C_{IO}	I/O and Output Capacitance	–	10	pF	

Note 1: These numbers apply for pins that do not have internal pull-up or pull-down resistors as shown in Table 139 .

Note 2: These numbers apply for pins that have internal pull-up or pull-down resistors as shown in Table 139 .

11.4 Interface Timing Specifications

The timing characteristics in this sub-section are given from the external devices' standpoint.



During AC testing, inputs are driven at 0.4V and 2.4V levels. Switching times are measured from the 1.4V level to the 0.8V or 2.0V levels at the input/output. If a figure shows timing from a mid-point, the timing is from 1.4V. If a figure shows timing from a level, the timing is from either 0.8V or 2.0V.

FIGURE 45. AC Testing Input, Output

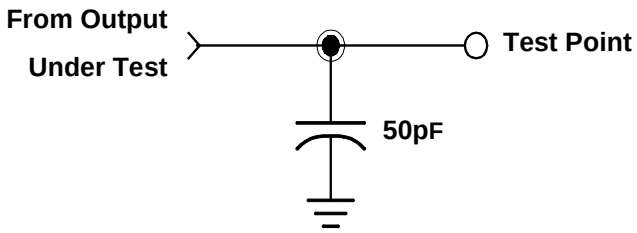


FIGURE 46. Normal AC Test Load

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11.4.1 Video Interface Timing

TABLE 85. Video Interface Timing @ 50pF Load

	Description	Min [ns]	Max [ns]	Comment
t_{VCH}	***VCLKx2*** high time	15		
t_{VCL}	***VCLKx2*** low time	15		
t_{VCR}	***VCLKx2*** rise time		3	
t_{VCF}	***VCLKx2*** fall time		3	
t_{VODM}	Output delay from ***VCLKx2***	6	21	Sync master mode
t_{VODS}	Output delay from ***VCLKx2***	10	28	Sync slave mode
t_{VCLKS}	***VCLK*** setup before ***VCLKx2***	12		Sync slave mode only.
t_{VCLKH}	***VCLK*** hold after ***VCLKx2***	0		Sync slave mode only.
t_{VIS}	Input setup before ***VCLKx2***	11		
t_{VIH}	Input hold after ***VCLKx2***	2		

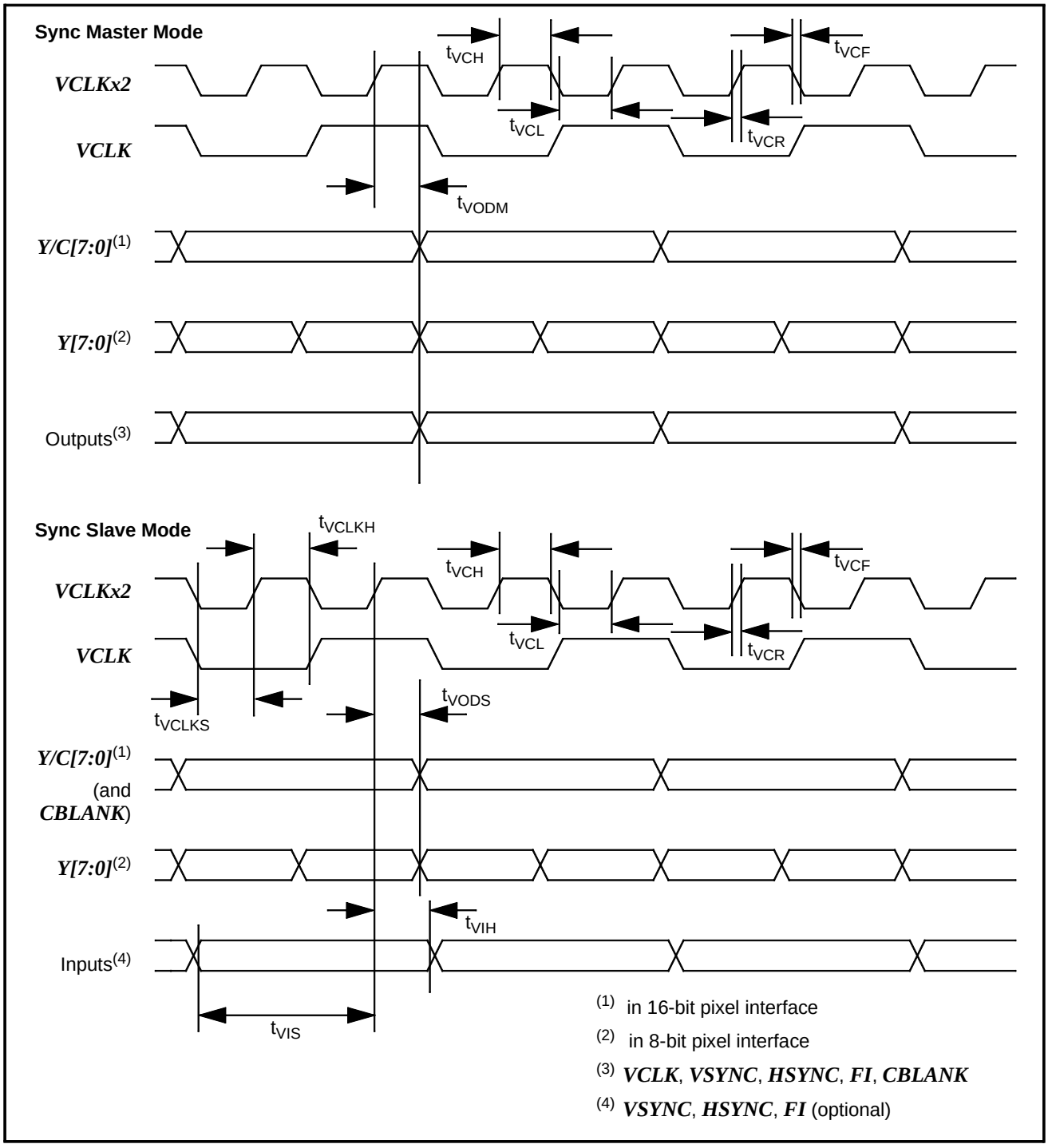

FIGURE 47. Video Interface Timing

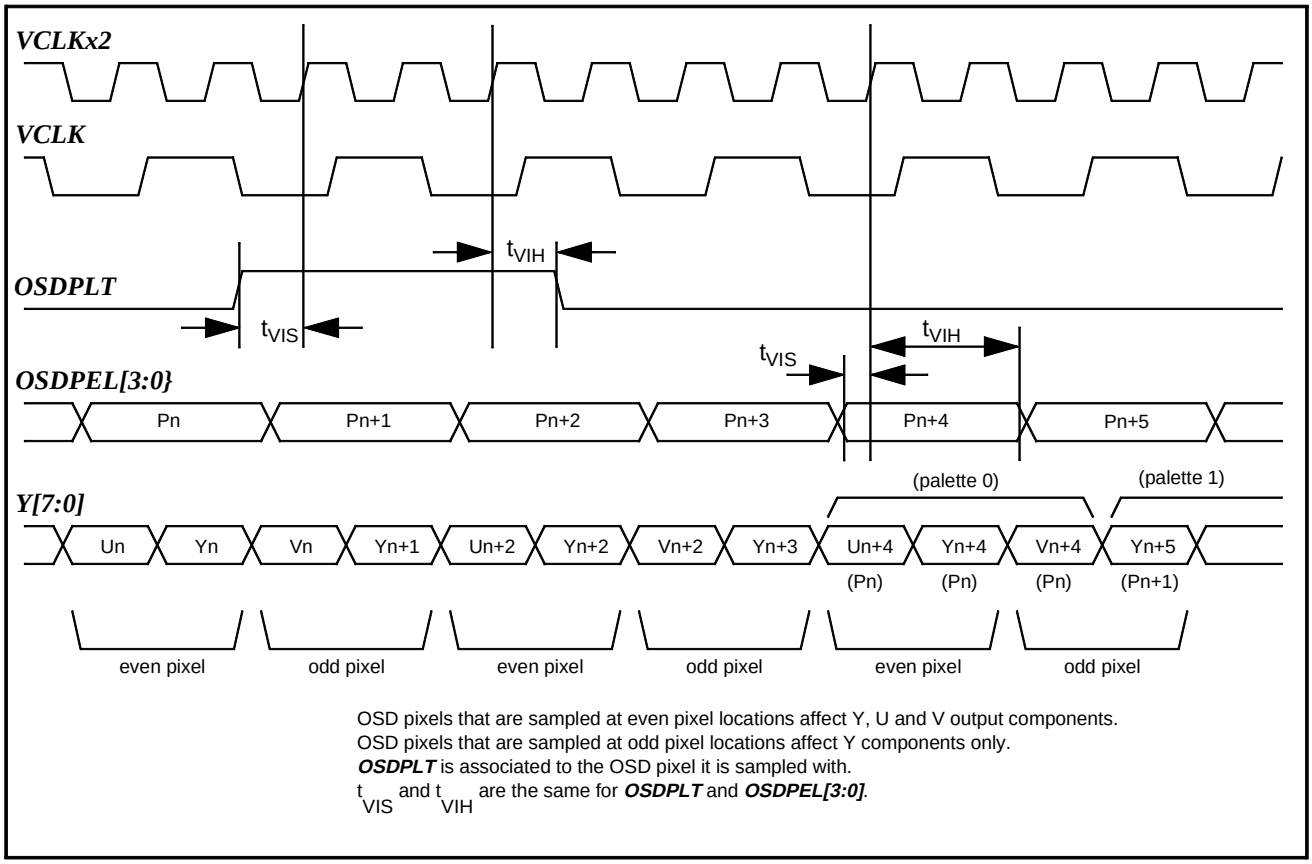

FIGURE 48. External OSD Interface Timing

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11.4.2 Host Interface Timing

TABLE 86. Host Interface Timing for Type A Protocol

	Description	Min [ns]	Max [ns]	Comment
t_{HA1}	***HCS#***, ***HA[3:0]***, ***HR/W#*** setup before ***HDS#*** negative edge	5		
t_{HA2}	***HCS#***, ***HA[3:0]***, ***HR/W#*** hold after ***HDS#*** negative edge	25		
t_{HA3}	***HACK#*** low delay after ***HDS#*** negative edge in write cycle	25	50	
t_{HA4}	***HDS#*** positive edge delay after negative edge of ***HACK#***	10	100	
t_{HA5}	Write cycle data setup before ***HDS#*** negative edge	5		
t_{HA6}	Write cycle data hold after ***HDS#*** positive edge	0		
t_{HA7}	***HACK#*** positive edge delay after positive edge of ***HDS#***	25	52	This may be called ***HACK#*** "hold time" after ***HDS#*** is de-asserted by the host.
t_{HA8}	Recovery (***HDS#*** high) after positive edge of ***HACK#*** (until next ***HDS#*** negative edge)	5		
t_{HA9}	***HACK#*** low delay after ***HDS#*** negative edge in read cycle	25	110	
t_{HA10}	Read cycle data setup before ***HACK#*** negative edge	10		
t_{HA11}	Read cycle data hold after ***HDS#*** positive edge	0	10	After 10ns the **ZR36710** must tri-state the ***HD*** lines.

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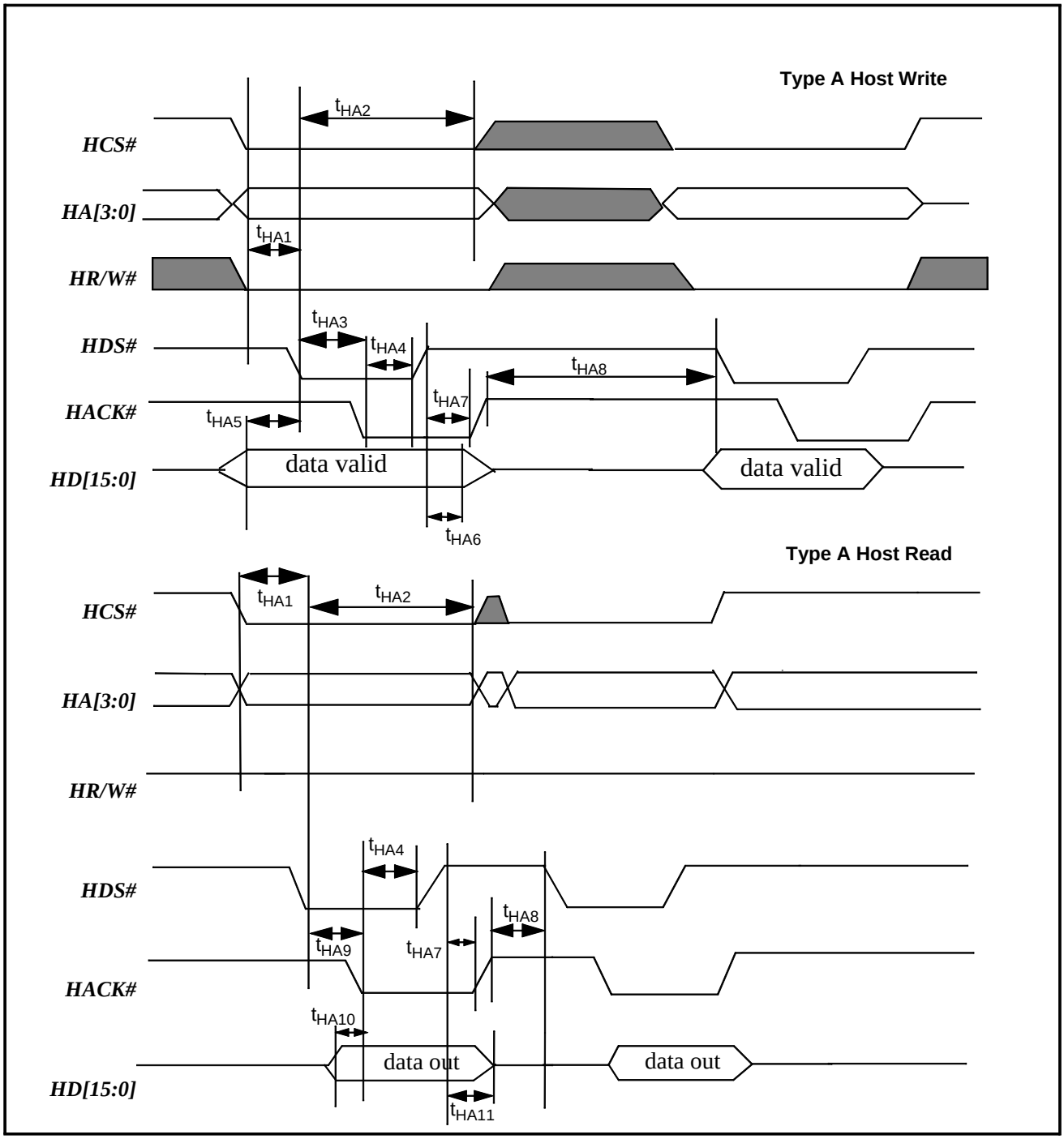


FIGURE 49. Host interface protocol - Type A.

TABLE 87. Host Interface Timing for Type B Protocol (both for using *HACK#* and not using *HACK#*)

	Description	Min [ns]	Max [ns]	Comment
t_{HB1}	***HCS#*** and ***HA[3:0]*** setup before ***HWR#*** or ***HRD#*** negative edge	10		
t_{HB2}	***HCS#*** and ***HA[3:0]*** hold after ***HWR#*** or ***HRD#*** negative edge	25		
t_{HB3}	Duration of ***HWR#*** low	40		See Figure 51. This value only matters if ***HACK#*** is not used.
t_{HB4}	***HACK#*** negative edge after ***HWR#*** or ***HRD#*** negative edge	0	15	***HACK#*** must be asserted fast enough to indicate the host to keep ***HWR#*** or ***HRD#*** asserted. See Figure 50. This value only matters if ***HACK#*** is used.
t_{HB5}	Recovery after ***HWR#*** or ***HRD#*** positive edge	38		
t_{HB6}	Duration of ***HACK#*** low in write cycle	25	50	See Figure 50. This value only matters if ***HACK#*** is used.
t_{HB7}	Data setup before ***HWR#*** positive edge	10		Data is sampled at the positive edge of the ***HWR#*** signal.
t_{HB8}	Data hold after ***HWR#*** positive edge	8		
t_{HB9}	Reserved			
t_{HB10}	Duration of ***HRD#*** low	100	*	See Figure 51. This value only matters if ***HACK#*** is not used. * As long as the host holds ***HRD#*** low, data will be valid.
t_{HB11}	***HACK#*** positive edge after ***HRD#*** negative edge	40	100	See Figure 50. This value only matters if ***HACK#*** is used.
t_{HB12}	Data output from **ZR36710** stable after ***HRD#*** negative edge	40	100	See Figure 51. This value only matters if ***HACK#*** is not used.
t_{HB13}	Data floats after ***HRD#*** positive edge		9	
t_{HB14}	***HWR#*** or ***HRD#*** positive edge after ***HACK#*** positive edge	0	*	See Figure 50. This value only matters if ***HACK#*** is used. * As long as the host holds ***HRD#*** low, data will be valid.
t_{HB15}	Data valid to ***HACK#*** positive edge	0		See Figure 50. This value only matters if ***HACK#*** is used.

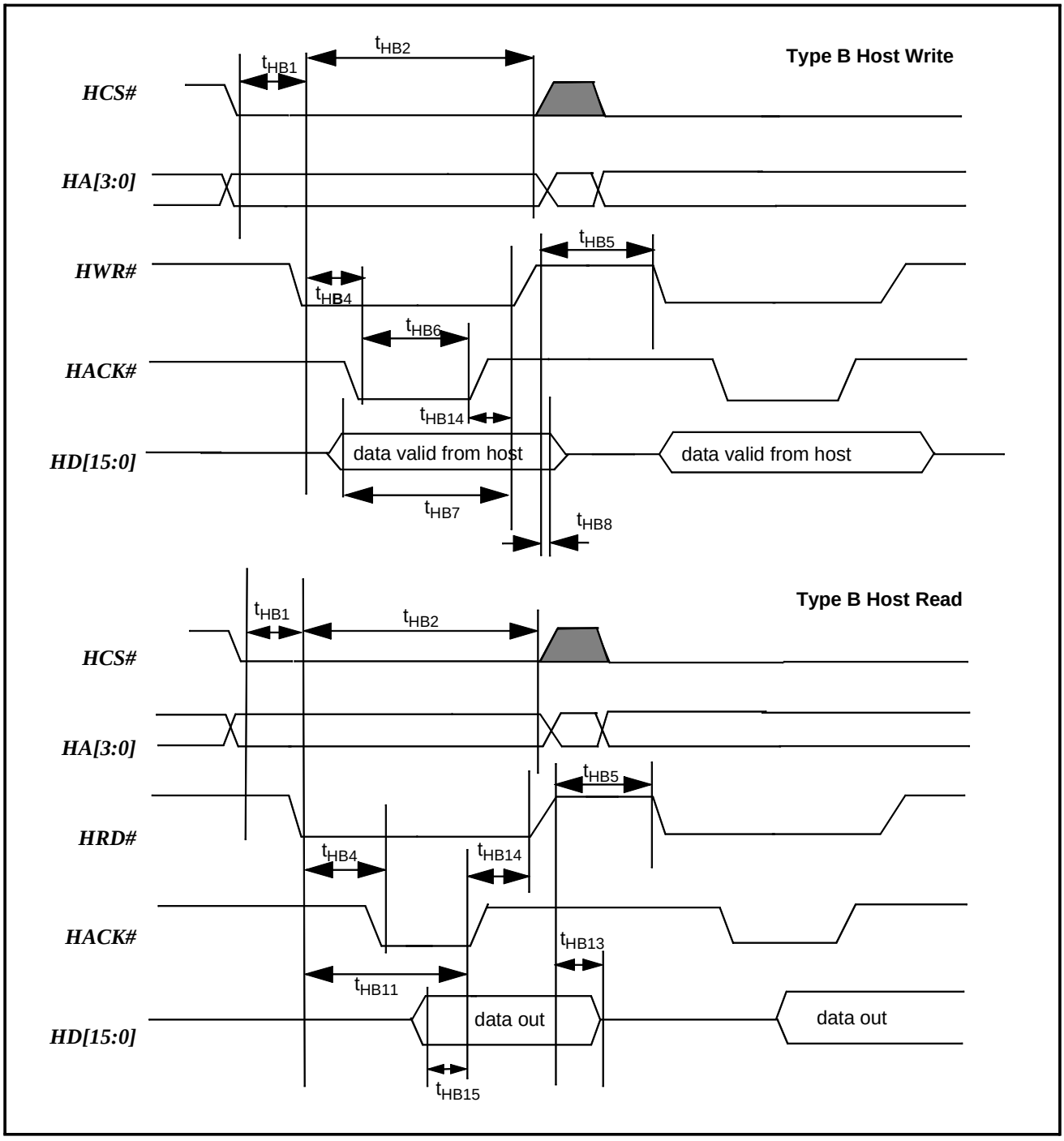


FIGURE 50. Host interface protocol - Type B, making use of HACK#.

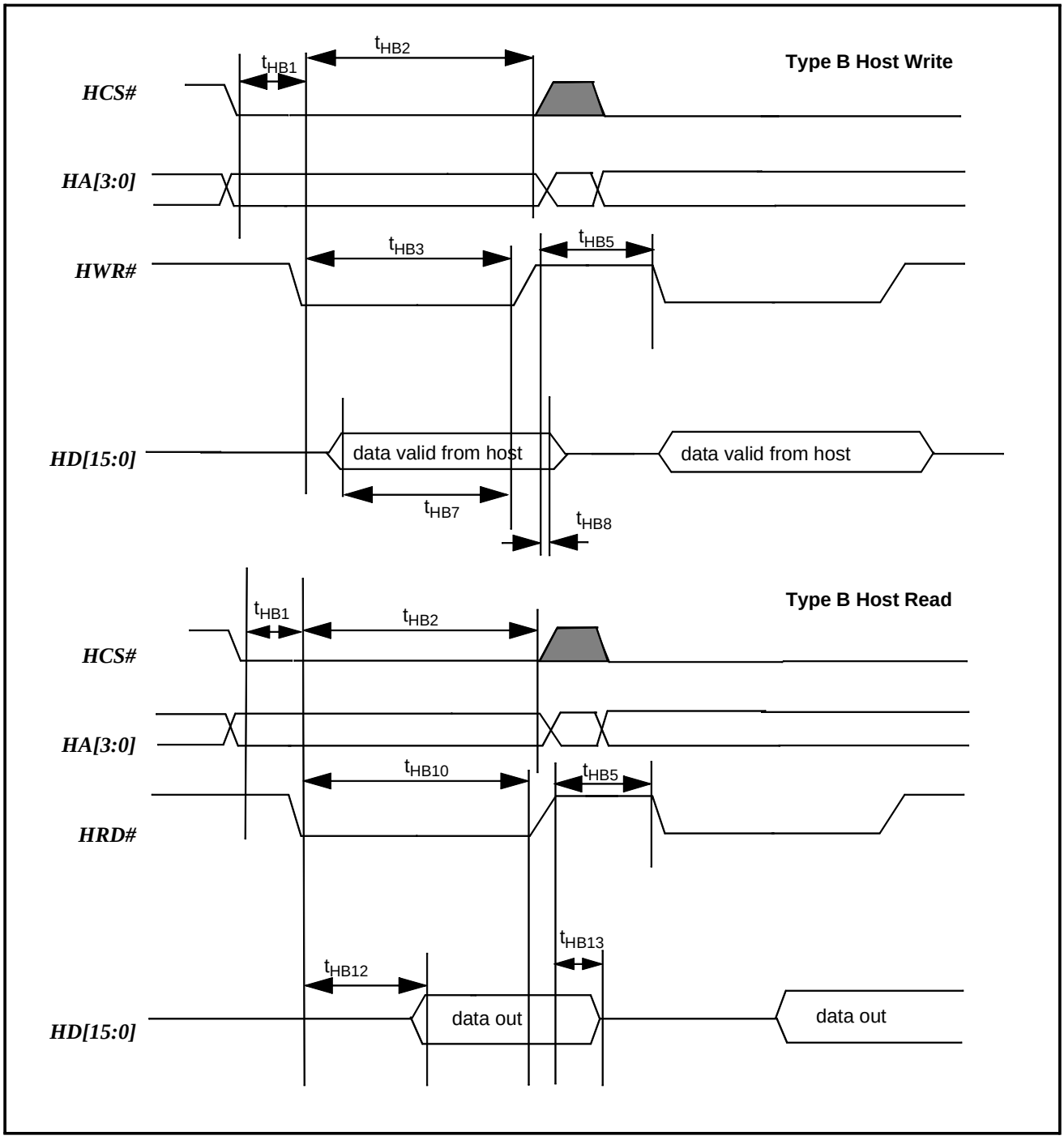
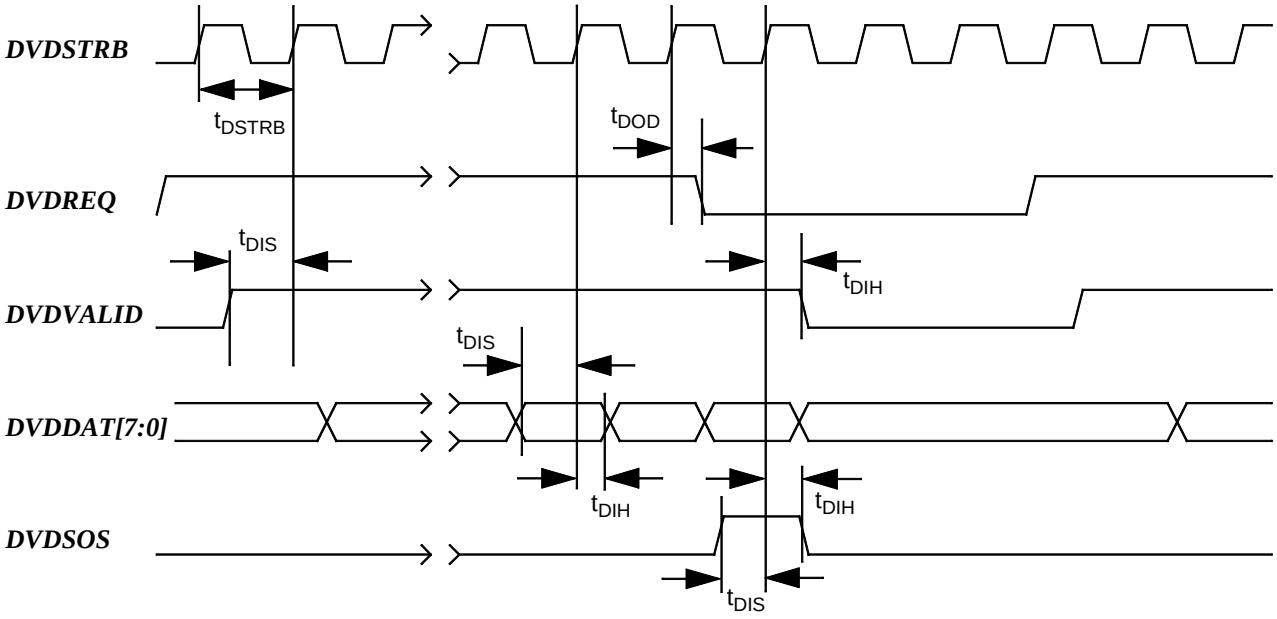


FIGURE 51. Host interface protocol - Type B, not using HACK#.

11.4.3 DVD-DSP Interface Timing

TABLE 88. DVD-DSP (parallel port) Timing

	Description	Min [ns]	Max [ns]	Comment
t_{DSTRB}	Time between two consecutive strobe sampling edges (either rising or falling as specified by the *STRBPol* bit of the *SDConfig* set-up parameter)	45		
t_{DOD}	***DVDREQ*** output delay after ***DVDSTRB*** sampling edge	0	15	Only applies when ***DVDREQ*** is synchronized with ***DVDSTRB*** (*DVDREQSync* = 1)
t_{DIS}	Input setup time before ***DVDSTRB*** sampling edge	9		
t_{DIH}	Output hold time after ***DVDSTRB*** sampling edge	3		



In this example:

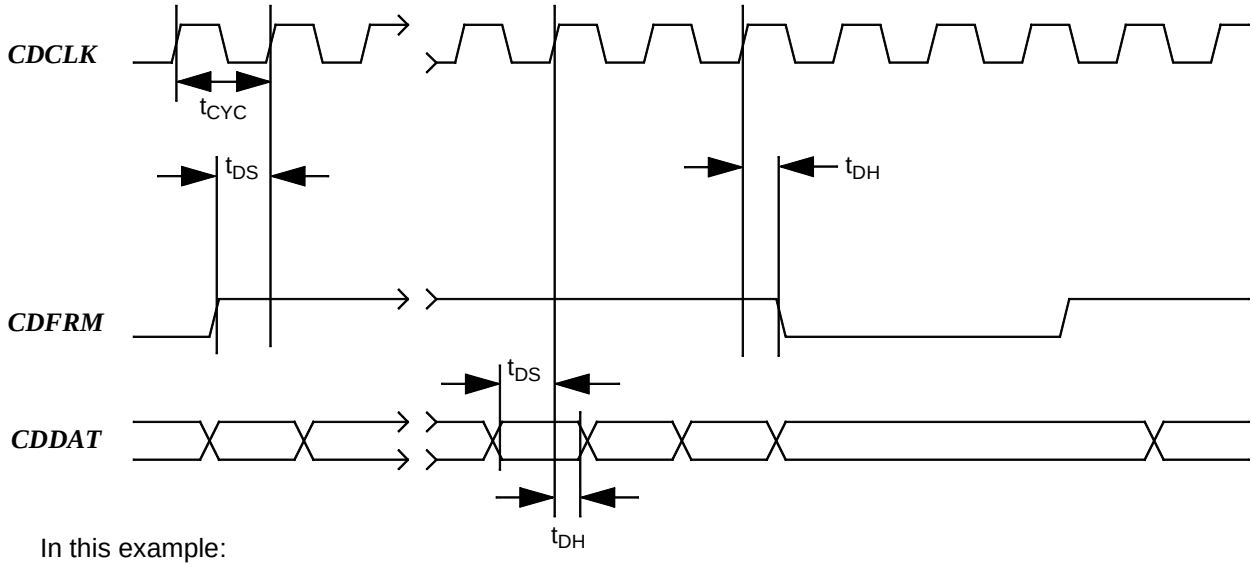
1. ***DVDSTRB*** is a clock signal, synchronous with ***DVDREQ***.
2. The polarity of ***DVDSTRB*** is configured positive (**ZR36710** samples with the positive edge of ***DVDSTRB***).
3. The polarities of ***DVDVALID***, ***DVDREQ*** and ***DVDSOS*** are configured positive, i.e., ***DVDVALID*** high means valid, ***DVDREQ*** high means the **ZR36710** requests data and ***DVDSOS*** high means start of sector.
4. The data source sends one additional code byte after the **ZR36710** de-asserts ***DVDREQ***.

FIGURE 52. DVD-DSP Parallel Port Timing

11.4.4 CD-DSP Interface Timing

TABLE 89. CD-DSP (VideoCD, CD-DA Serial Port) Timing

	Description	Min [ns]	Max [ns]	Comment
t_{cyc}	***CDCLK*** period	5 PCLK periods*		*5 PCLK periods at 81MHz = 62ns
t_{DS}	Setup time before ***CDCLK***	10		
t_{DH}	Hold time after ***CDCLK***	5		



In this example:

1. The polarity of ***CDCLK*** is configured positive. (**ZR36710** samples with the positive edge of ***CDCLK***).

FIGURE 53. CD-DSP Serial Port Timing

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11.4.5 Audio Interface Timing

TABLE 90. Audio Port Timing

	Description	Min [ns]	Max [ns]	Comment
t_{AUD0}	***AMCLK*** period	27		
t_{AUD1}	***AMCLK*** high width	45%	55%	Percentage of duty cycle of ***AMCLK***
t_{AUD2}	***AMCLK*** low width	45%	55%	Percentage of duty cycle of ***AMCLK***
t_{AUD3}	***ABCLK*** period	50		
t_{AUD4}	***ABCLK*** high width	45%	55%	Percentage of duty cycle of ***ABCLK***
t_{AUD5}	***ABCLK*** low width	45%	55%	Percentage of duty cycle of ***ABCLK***
t_{AUD6}	***AOUT*** and ***ALRCLK*** delay time from ***ABCLK***		25	Measured from selected sampling edge of ***ABCLK***.
t_{AUD7}	***AIN*** setup time before ***ABCLK***	15		Measured to selected sampling edge of ***ABCLK***.
t_{AUD8}	***AIN*** hold time after ***ABCLK***	15		Measured from selected sampling edge of ***ABCLK***.

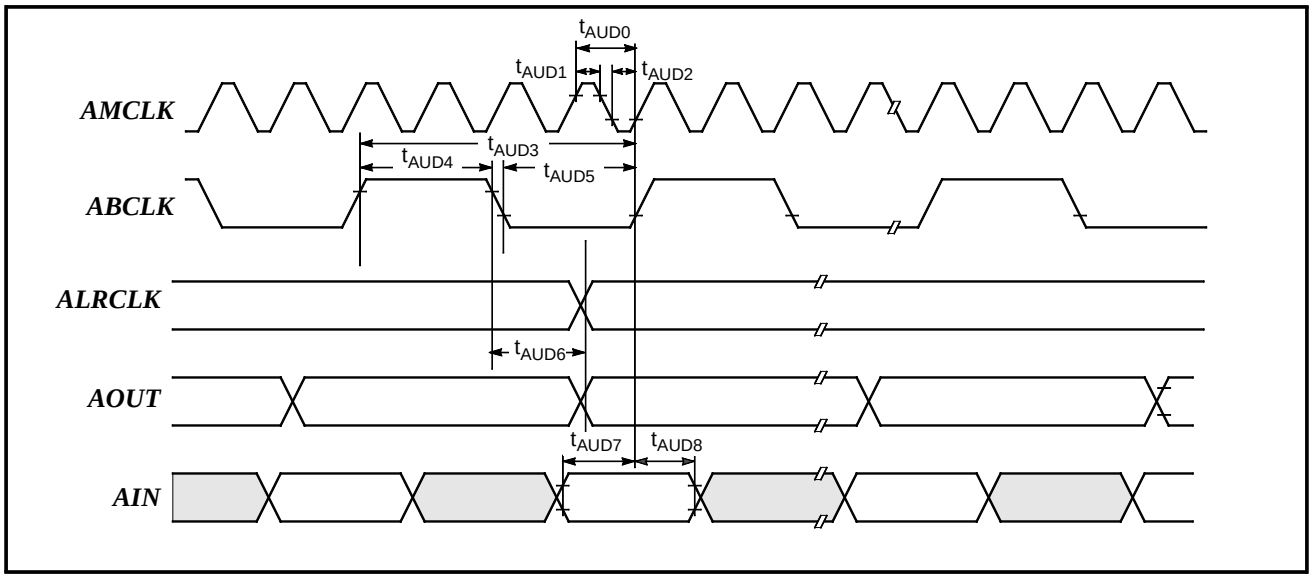

FIGURE 54. Audio Port Timing

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11.4.6 SDRAM Interface Timing

The SDRAM interface timing are designed to fit 16 Mbit SDRAM devices of the "-10" type manufactured by Toshiba, Samsung, NEC and Hitachi.

TABLE 91. SDRAM interface timing

	Description	Min [ns]	Max [ns]	Comment
t_{OD}	Output delay	2	8.3	
t_{IH}	Input hold	1		
t_{IS}	Input set-up	3.5		
t_{TR}	Transition time		1	20 pF load
t_{PCH}	***PCLK*** high	4		
t_{PCL}	***PCLK*** low	4		

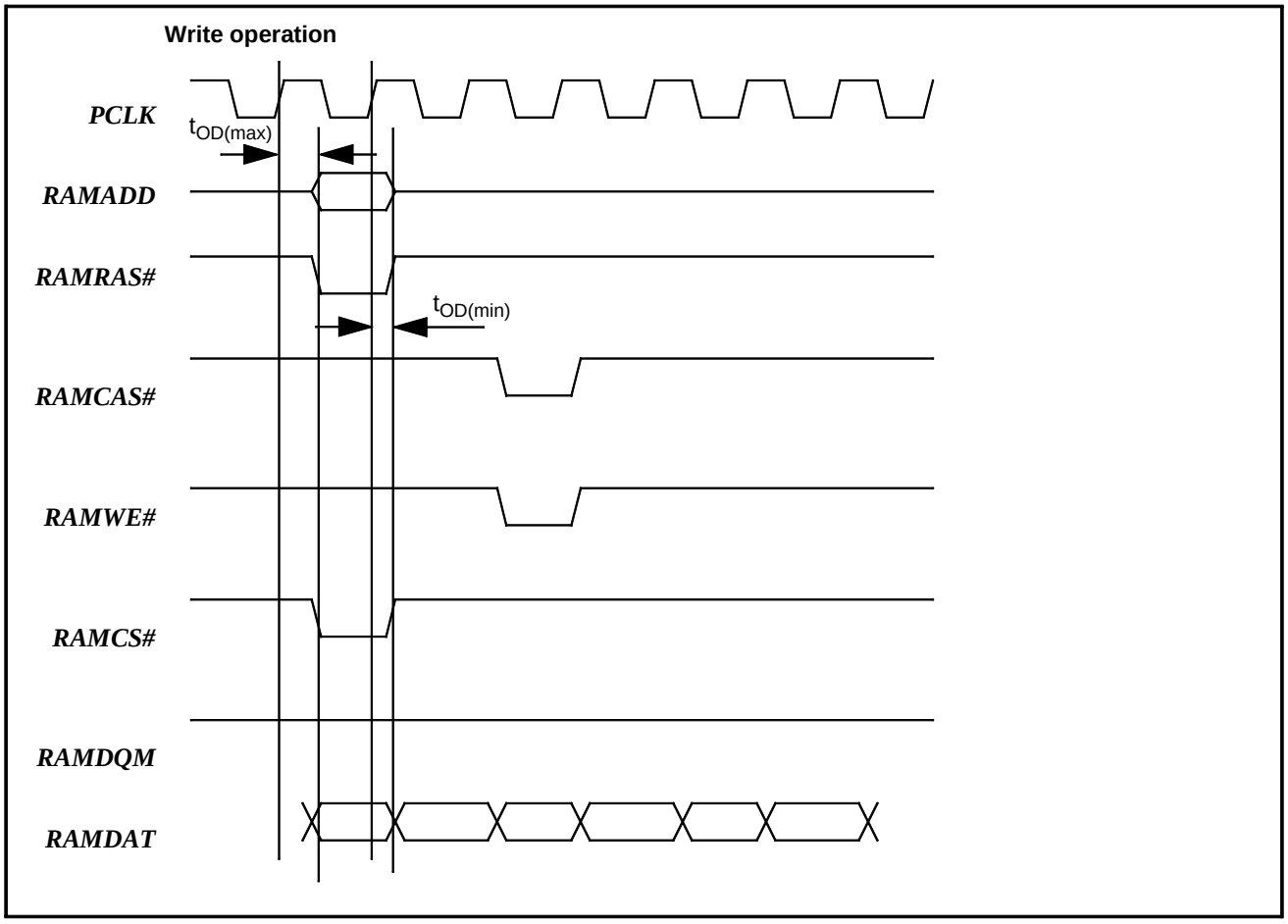

FIGURE 55. SDRAM Interface Write Operation Timing

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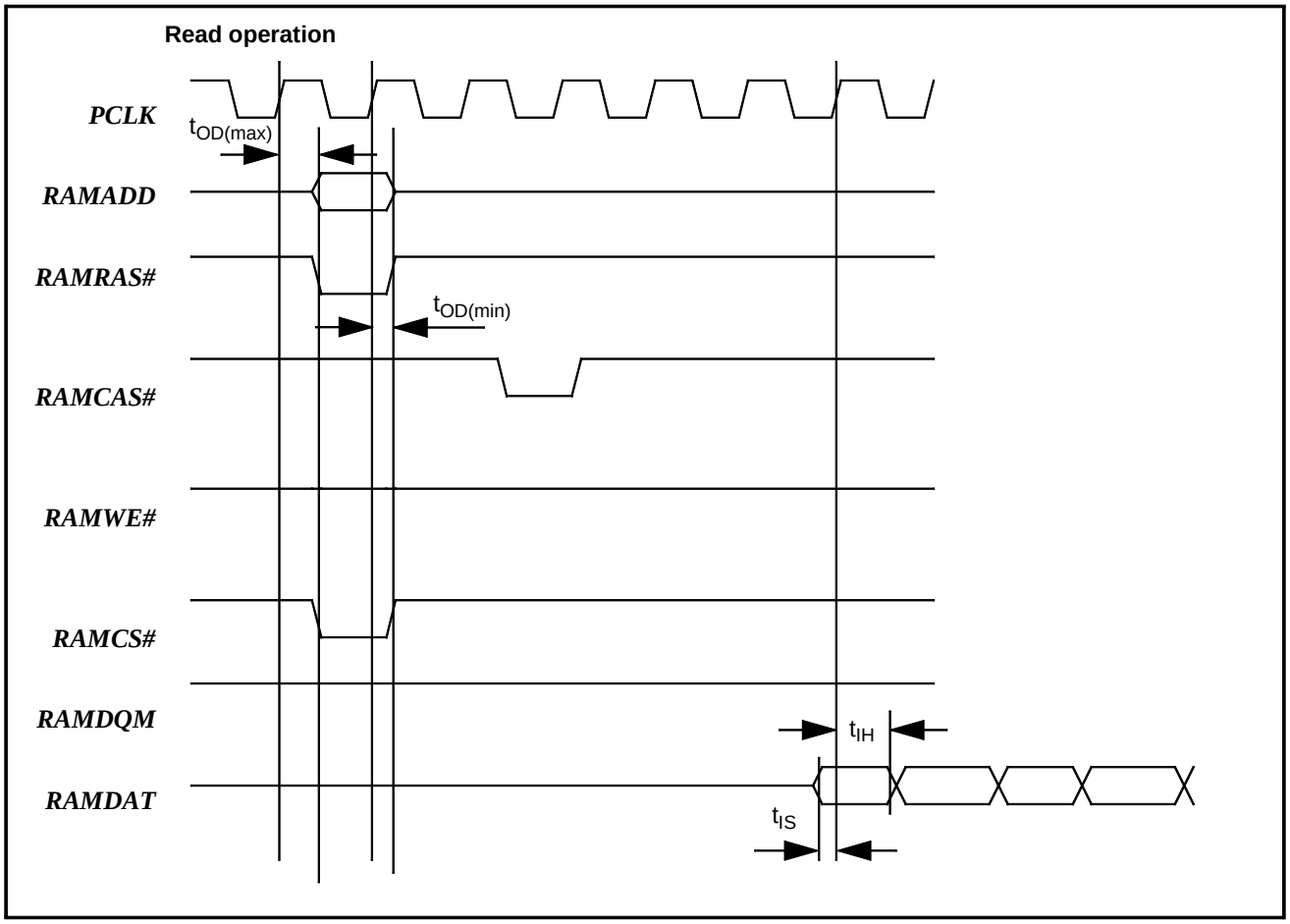

FIGURE 56. SDRAM Interface Read Operation Timing

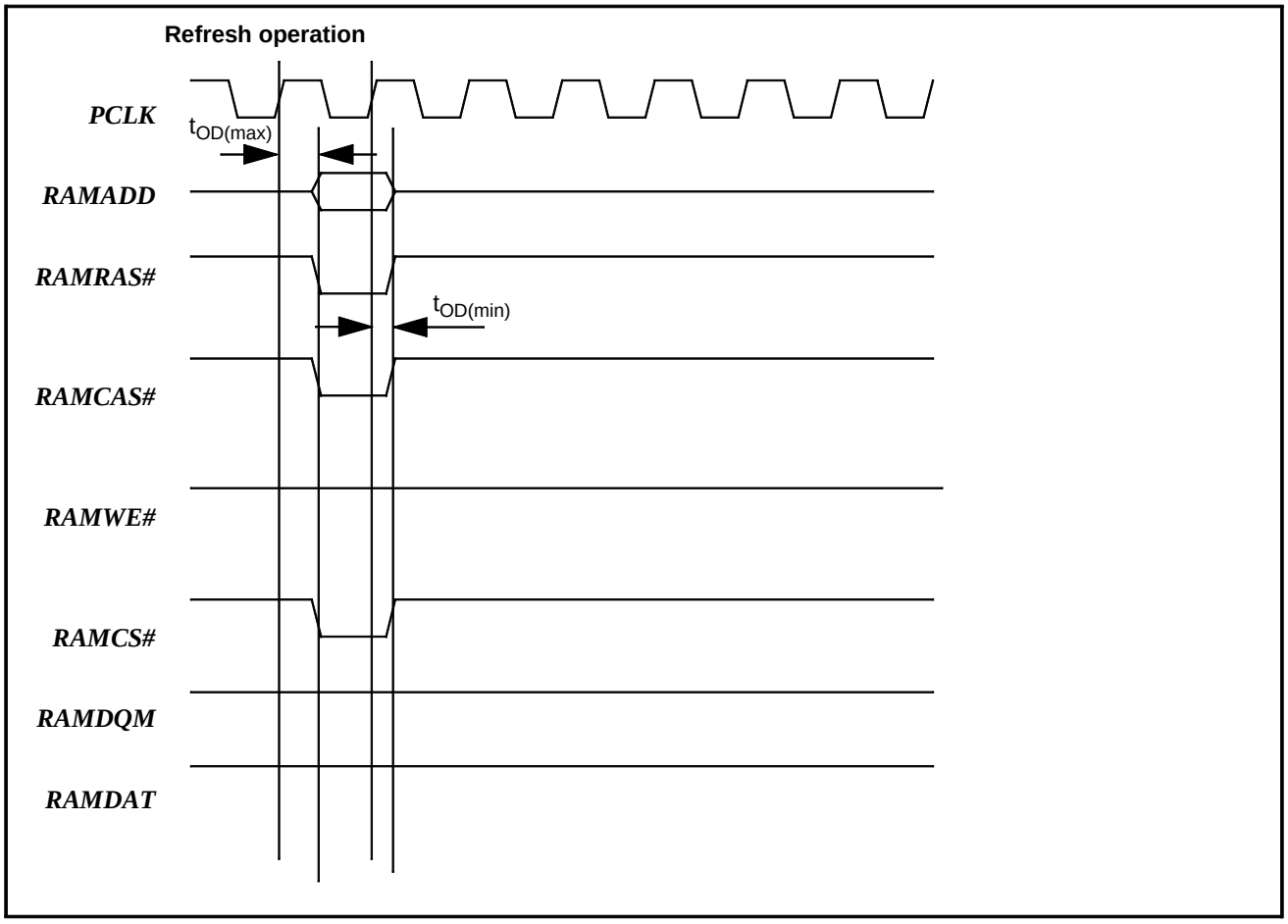

FIGURE 57. SDRAM Interface Refresh Operation Timing

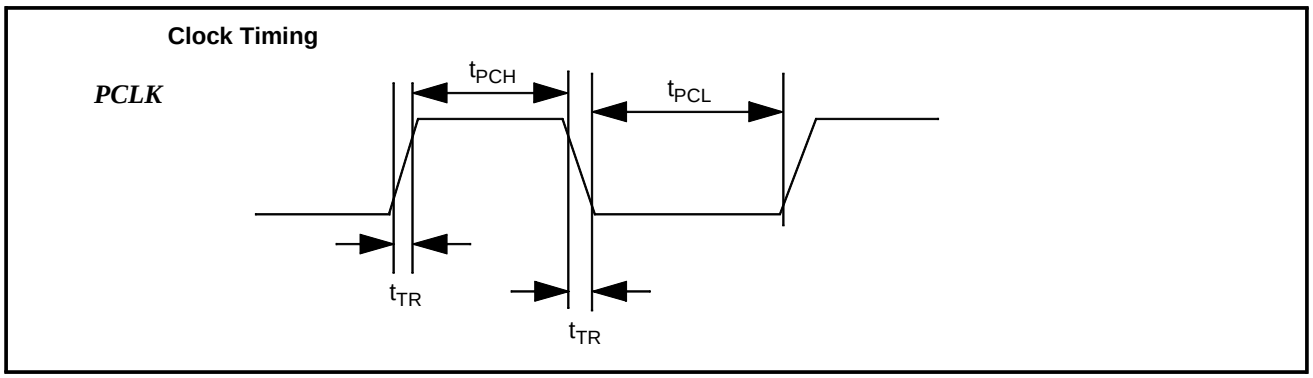

FIGURE 58. SDRAM Clock Timing

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11.4.7 PLL Interface Timing

TABLE 92. PLL Interface Timing @ 50pF Load

	Description	Min [ns]	Max [ns]	Comment
t_{GCP}	***GCLK*** period	37		(27 MHz nominal)
t_{GCH}	***GCLK*** high time	10		
t_{GCL}	***GCLK*** low time	10		
t_{GCR}	***GCLK*** rise time		1.5	
t_{GCF}	***GCLK*** fall time		1.5	
t_{GC1P}	***GCLK1*** period	37		(27 MHz nominal)
t_{GC1H}	***GCLK1*** high time	10		
t_{GC1L}	***GCLK1*** low time	10		
t_{GC1R}	***GCLK1*** rise time		1.5	
t_{GC1F}	***GCLK1*** fall time		1.5	

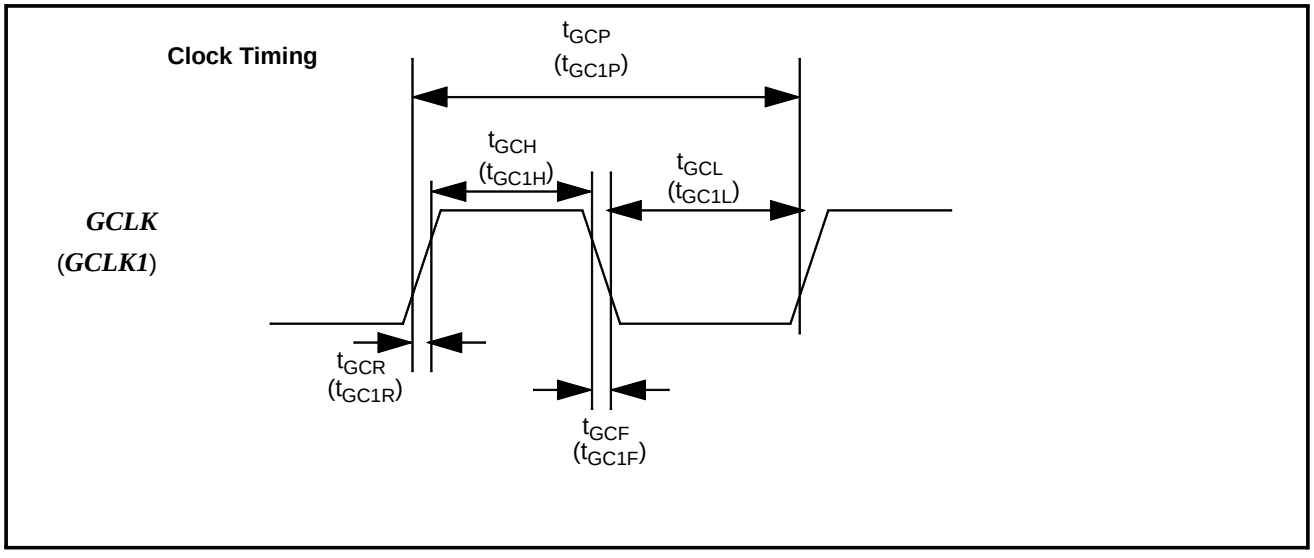

FIGURE 59. *GCLK* and *GCLK1* Timing

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12. Annex A: ADP Commands

This section explains the ADP command interface of the **ZR36710**. Through this interface, the host can download microcode to the ADP, configure the audio output port, configure the audio input port, select audio sampling rates, configure the decoding parameters of the ADP and take advantage of several other features the ADP offers.

12.1 ADP Command Overview

Section 5.8 “ADP Access - Reg. 0x8” explains the protocol between the host and the **ZR36710** for communication with the ADP. Each ADP command is a byte or a sequence of bytes. The first byte is the “opcode” byte, identifying the operation. If required, the opcode byte is followed by a variable number of “parameter” bytes.

12.1.1 ADP Command List

Table 93 specifies the legal ADP commands, giving the opcode byte value, the number of parameters and the function of the command.

TABLE 93. Command codes and parameters

Opcode byte	Number of parameter bytes	Mnemonic	Description
0x00	0	READ	read response
0x80	0	NOP	no operation
0x81	0	VER	read ADP ROM version
0x82	8	CFG	Audio interface (I/F) configuration setting
0x83	8	PINK	Pink noise generator function selection
0x84	8	LPCM/DTS	DVD PCM function selection or DTS S/PDIF function selection
0x85	8	AC3	Dolby AC-3 function selection
0x86	8	PCM	CD-DA stereo function selection
0x87	8	MPEG	MPEG function selection
0x88	8		reserved
0x89	0	UNMUTE	disable mute
0x8A	0	PLAY	start, or resume play after STOP
0x8B	0	MUTE	mute
0x8C	0	STOP	stop decoding
0x8D	0	STOPF	stop decoding and flush buffers
0x8E	0	STAT	read status information
0x90	N	BOOT	load program to ADP RAM
0x91	4	INTRP	interpret an ADP instruction
0x92	4	SETIO	set/test programmable GPIOA pins
0x93	8+4*size	POKE	write an ADP RAM block of specified size elements

TABLE 93. Command codes and parameters

Opcode byte	Number of parameter bytes	Mnemonic	Description
0x94	7	PEEK	read an ADP RAM block of specified size elements starting at the specified address
0x95	4	SPDIFCS	S/PDIF channel status setting
0x96	1+3*N	PARAM	user parametric command
0x98	6	PLLTAB	PLL programming command
0x99	1	PLLCFG	PLL configuration command

12.1.2 Support of Current and Future ADP Commands - Microcode Releases

The list of supported ADP commands shown in Table 93 can be expanded upon as new versions of ADP microcode are released. As new releases of microcode are made available, the accompanying release notes will explain any new ADP commands that are supported in the release.

The specification of the current ADP commands explained in this section can be changed by future microcode releases. As new releases of microcode are made available, the accompanying release notes will explain any changes to the current ADP command specifications.

12.1.3 ADP Command Structure

The host transfers each byte of the ADP command to the ADP Data Register. For each byte transferred from the host, the ADP returns a byte to the host. This returned byte is available via the ADP Status Register.

The response byte is always one ADP command “late”. For example:

- Host writes ADP command “X”. Host reads ADP response byte for ADP command “X - 1”.
- Host writes ADP command “X + 1”. Host reads ADP response byte for ADP command “X”.

There are three types of the ADP response bytes:

- **ISTATUS**: This is the response byte for the opcode byte. This indicates if the current ADP command was handled properly by the ADP. The legal values of this response are given in the following table.

TABLE 94. ADP command interpreter status (**ISTATUS**)

Previous Command Status	Value
no error	0x80
opcode error	0x81
EXT parameter error (for the PARAM command)	0x82
not ready for new command	0x83
reserved	0x84
ready for new command	0x85

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Only after ALL the parameter bytes (if any) have been entered can the ADP return the ISTATUS byte. If an error occurred while writing the opcode byte (0x81), ISTATUS is returned with the next byte written by the host.

- **Count** of the bytes still required to complete the command: The returned byte from the ADP shows the number of command bytes (including the opcode and parameter bytes) still expected to be transferred to the ADP. The last expected number is followed by ISTATUS. The last number prior to ISTATUS is 1. Figure 60 shows how an ADP command with five parameter bytes is entered and what bytes are returned until ISTATUS is read. A READ command must be used to extract the ISTATUS byte.

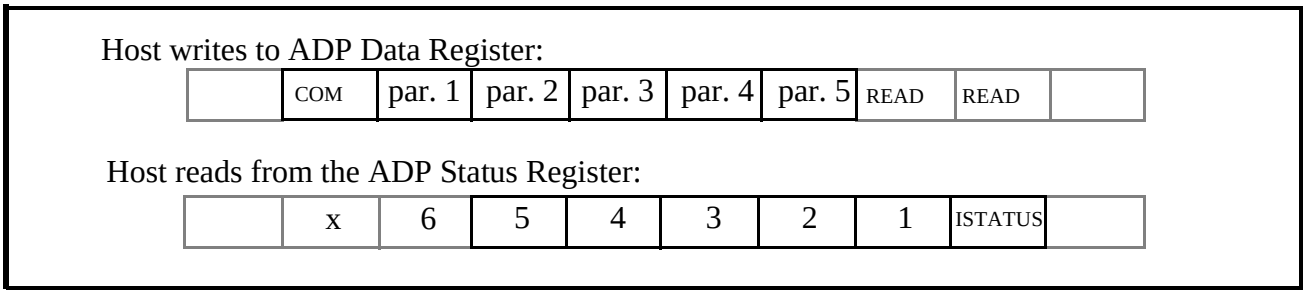

FIGURE 60. The number of bytes left to write always lags by 2.

In Figure 60, COM stands for an ADP command opcode byte, and Par.*i* stands for parameter byte number i.

- **ADP Status**: Some ADP commands (e.g. STAT) require the ADP to return data values (one or more bytes) to the ADP Status register. After decoding the ADP command, the ADP prepares the information in a buffer. To retrieve the data, multiple READ commands are issued and the ADP returns one byte for each READ command. After all response bytes are given by the ADP, the ISTATUS response is issued on the next READ command. Figure 61 gives an example (the SETIO command), which has 4 parameters bytes and 2 response bytes.

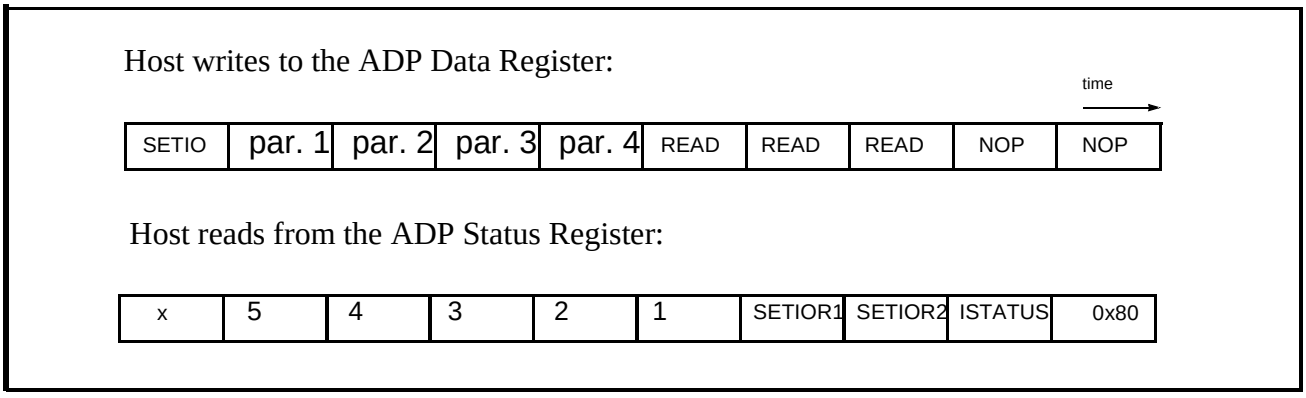

FIGURE 61. Retrieving status bytes for ADP commands that return status bytes.

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In Figure 61, SETIOR1 and SETIOR2 are the reply bytes from the ADP. The value 0x80 is returned as the ISTATUS response to an NOP command.

There are two classes of ADP commands: Those that write to the ADP and those that read back from the ADP. The write commands are of four types:

- Function selection.
- Operation control (e.g. STOP or PLAY).
- Set up the ADP for operation (e.g. CFG).
- Microcode loading and debug.

The read commands fall under one type:

- Status (STAT).

The description of the commands can be found in the following sections. In the description of the command parameters, only legal values are mentioned. All other values are reserved and must not be used.

12.2 Function Selection Commands

The commands in this group are AC3, PCM, LPCM, MPEG, DTS and PINK.

If the audio is muted via the MUTE ADP command as explained in Section 12.3 “Operation Control Commands”, these function selection commands will unmute the audio. If the audio needs to restore the mute condition, then the host must reissue a MUTE ADP command after issuing the appropriate function selection command.

12.2.1 AC3

This command selects the AC-3 function. Prior to calling this function, the host must load one of two ADP microcodes (refer to microcode release notes), depending on whether the output is 2-channels or 6-channels. Two-channel mode allows for either down-mixing of a multi-channel bitstream or 3D processing. Two-channel mode also supports S/PDIF output and microphone mixing. Six-channel mode supports bass redirection and Dolby Pro Logic. Both modes support Karaoke processing. Please refer to the Dolby Licensing Manual Version 1.0 dated October 1995 for more information regarding the definition of the bits within this command.

TABLE 95. AC3 Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00101b**				
parameter 1	PRLG		00b		COMP		DMM	
parameter 2	SF	AB	BCFG		SW	OCFG		
parameter 3	CDLY		SRDLY					
parameter 4	HDYNRNG							
parameter 5	LDYNRNG							
parameter 6	0000b				KAR	RPC		
parameter 7	PCMSF (m.s.)							
parameter 8	PCMSF (l.s.)							

TABLE 96. Parameter Description - AC3

Parameter	Description	Values
PRLG	Dolby Pro Logic mode	(00b) No Pro Logic decoding (01b) Pro Logic decoding - Note 1 (10b) Automatic Pro Logic decoding (determined if bitstream indicates the Pro Logic decoding is allowed) - Note 1 (11b) Reserved
COMP	compression mode	(00b) Custom 0 (01b) Custom 1 (10b) Line mode (11b) RF

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Phone (408) 919-4111 Fax (408) 919-4122

TABLE 96. Parameter Description - AC3

Parameter	Description	Values
DMM	dual mono reproduction mode	(00b) L channel to left output R channel to right output (01b) L channel to left and right outputs (10b) R channel to left and right outputs (11b) ((R + L) / 2) to left and right outputs
SF	Dolby Pro Logic surround filter (NR and LP filter)	(0) filters active - Note 1 (1) filters inactive
AB	auto balance (Dolby Pro Logic, only)	(0) effective - Note 1 (1) not effective
BCFG	bass redirection configuration	(00b) not effective (01b) redirect to left and right - Note 1 (10b) reserved (11b) redirect to subwoofer - Note 1
SW	sub-woofer output channel	(0) no subwoofer (1) present - Note 1
OCFG	output speaker configuration	(000b) 2/0 down-mix (Dolby Pro-Logic compatible) (001b) 1/0 (requires DMM = 01b) (010b) 2/0 without down-mix (011b) 3/0 - Note 1 (100b) 2/1 - Note 1 (101b) 3/1 - Note 1 (110b) 2/2 - Note 1 (111b) 3/2 - Note 1
CDLY	center channel delay (0 - 5ms) in 1ms steps	(0) No delay or not applicable (2-channel) (1 - 5) 1 - 5ms - Note 1
SRDLY	surround delay channel (0 - 15ms) in 1ms steps	For 2-channel mode: (0) disable 3D (16) enable 3D For 6-channel mode: (0 - 15) 0 - 15ms (without Dolby Pro Logic) (0 - 15) 15 - 30ms (with Dolby Pro Logic) (16) No delay (with Dolby Pro Logic)
HDYNRNG	dynamic range scale factor for high level signals	Note 2
LDYNRNG	dynamic range scale factor for low level signals	Note 2
KAR	Karaoke Mode	(0) disabled (1) enabled - Note 3
RPC	maximum repeat count before muting	(0 - 7)
PCMSF (m.s.)	output scale factor (most significant byte)	(0x0000) min gain to (0x7FFF) max gain
PCMSF (l.s.)	output scale factor (least significant byte)	

Note 1: Is not supported in 2-channel mode and therefore must not be set to this value.

Note 2: 0x00 for no effect of bitstream dynamic compression parameters to 0x7F for full effect.

Note 3: If Karaoke mode is enabled, then the host must write the PARAM (EXT = 0x04) ADP command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 4: The SPO bit in the CFG command must be 0 if 6-channel mode is enabled.

Note 5: If bass redirection is enabled (6-channel mode only), the bass redirection attenuation is set by the PARAM (EXT = 0x05) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 6: To enable microphone mixing (2-channel mode only), the host must write the PARAM (EXT = 0x06) ADP command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 7: The 3D setting can be changed during playback by a PARAM (EXT = 0x01) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

12.2.2 PCM

This command selects the stereo PCM function for CD-DA discs. Prior to calling this function, the host must load a CD-DA ADP microcode (refer to microcode release notes). If voice extraction and/or microphone mixing is required, after the host writes this command, the host must write the voice extraction/microphone scaling control via the PARAM ADP command as explained in Section 12.4.1 “Special Function Parameter Command (PARAM)”. 3D processing is also supported in this mode.

TABLE 97. PCM Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00110b**				
parameter 1	PRLG		SI	000b				DMM
parameter 2	SF	AB	BCFG		SW	OCFG		
parameter 3	CDLY			SRDLY				
parameter 4	00000000b							
parameter 5	00000000b							
parameter 6	00b		VE		0000b			
parameter 7	PCMSF (m.s.)							
parameter 8	PCMSF (l.s.)							

TABLE 98. Parameter Description - PCM

Parameter	Description	Values
PRLG	Pro Logic mode	(00b) off (01b) on (10b, 11b) reserved
SI	serial data input	(0) Input data through host, CD-DSP or DVD-DSP interface. (1) Input data through ***AIN*** pin.
DMM	dual mono reproduction mode	(00b) L channel to left output R channel to right output (01b) L channel to left and right outputs (10b) R channel to left and right outputs (11b) ((R + L) / 2) to left and right outputs
SF	Dolby Pro Logic surround filter (NR and LP filter)	(0) filters active (1) filters inactive
AB	auto balance (Dolby Pro Logic, only)	(0) effective (1) not effective
BCFG	bass redirection configuration	(00b) not effective (01b) redirect to left and right (10b) reserved (11b) redirect to subwoofer

TABLE 98. Parameter Description - PCM

Parameter	Description	Values
SW	sub-woofer output channel	(0) no subwoofer (1) subwoofer present
OCFG	output speaker configuration (Pro Logic decoding may be automatically performed for an output configuration greater than 2 channels)	If PRLG = 0 or 3D is on, then all values for OCFG will indicate 2/0 without down-mix. If PRLG = 1 and 3D is off, then the following apply: (000b) reserved (001b) reserved (010b) reserved (011b) 3/0 (100b) 2/1 (101b) 3/1 (110b) 2/2 (111b) 3/2
CDLY	center channel delay (0 - 5ms) in 1ms steps	(0 - 5) 0 - 5ms (0) for 3D sound
SRDLY	surround delay channel (0 - 15ms) in 1ms steps	(0 - 15) 0 - 15ms (without Dolby Pro Logic) (0 - 15) 15 - 30ms (with Dolby Pro Logic) (16) No delay (with Dolby Pro Logic) or 3D sound is active.
VE	voice extractor flags	(00b) no voice extractor (01b) voice extractor for Music CD (10b) reserved (11b) voice extractor for Karaoke CD
PCMSF (m.s)	output scale factor (most significant byte)	0x0000 min gain to 0x7FFF max gain
PCMSF (l.s.)	output scale factor (least significant byte)	

Note 1: Bass redirection attenuation is controlled by the PARAM (EXT = 0x05) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 2: If 3D is on (CDLY = 0 and SRDLY = 16), the output will always be 2/0 regardless of the OCFG value.

Note 3: If 3D is on, crossover will not be executed regardless of the BCFG value.

Note 4: The 3D setting can be changed during playback by a PARAM (EXT = 0x01) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 5: If a voice extractor mode is enabled, then the PARAM (EXT = 0x06) command must be sent.

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Phone (408) 919-4111 Fax (408) 919-4122

12.2.3 LPCM

This command selects the DVD PCM (8-channel) decoder function. Prior to calling this function, the host must load LPCM ADP microcode (refer to the microcode release notes). If custom channel downmixing is required, after the host writes this command, the host must write the custom downmix table via the PARAM ADP command as explained in Section 12.4.1 “Special Function Parameter Command (PARAM)”. 3D processing is also available in this mode.

TABLE 99. LPCM Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00100b**				
parameter 1	PRLG		000b			DE	00b	
parameter 2	SF	AB	BCFG		SW	OCFG		
parameter 3	CDLY		SRDLY					
parameter 4	DRC							
parameter 5	00000000b							
parameter 6	CMX	0000000b						
parameter 7	PCMSF (m.s.)							
parameter 8	PCMSF (l.s.)							

TABLE 100. Parameter Description - LPCM

Parameter	Description	Values
PRLG	Dolby Pro-Logic enable flag	(0) disabled (1) enabled unconditionally if input is stereo (2, 3) reserved
DE	de-emphasis flag enable	(0) no flag (1) GPAIO0 is set if bitstream is pre-emphasized
SF	Dolby Pro Logic surround filter (NR and LP filter)	(0) enabled (1) LP + NR disabled
AB	auto balance	(0) enabled (1) disabled
BCFG	bass redirection configuration	(0) no redirection (1) redirect to left and right (2) reserved (3) redirect to subwoofer
SW	sub-woofer present flag	(0) missing (1) present

TABLE 100. Parameter Description - LPCM

Parameter	Description	Values
OCFG	output speaker configuration	(0) 5/2 -> 7.1 channels (1) 1/0 -> mono to center if PRLG = 1 (2) 2/0 -> stereo (3) 3/0 (4) 2/1 (5) 3/1 (6) 2/2 (7) 3/2
CDLY	center channel delay (0 - 5ms) in 1ms steps	(0 - 5) 0 - 5ms (0) for 3D sound
SRDLY	surround channel delay (0 - 15ms) in 1ms steps	(0 - 15) 0 - 15ms. A 15ms delay is automatically added to the specified value for Pro Logic. (16) no delay, 3D sound is active.
DRC	dynamic range control scale factor	(0x00 - 0x7F) no control - full control. PCM gain = 2^((4-X+Y/30))*DRC, X,Y in input stream
CMX	channels mixing flag	(0) use default tables for OCFG = 2 (1) use channel downmix table for custom downmix (see Section 12.4.1)
PCMSF (m.s.)	output scale factor (most significant byte)	0x0000 min gain to 0x7FFF max gain
PCMSF (l.s.)	output scale factor (least significant byte)	

Note 1: If 3D and Pro Logic are active, OCFG indicates the number of channels on the Pro Logic output, which is the input to 3D.

Note 2: If 3D is active, the output is always 2 channel, regardless of the OCFG value.

Note 3: In 7.1 mode (OCFG = 0), Pro Logic and crossover cannot be active.

Note 4: The 3D setting can be changed during playback by a PARAM (EXT = 0x01) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 5: Bass redirection attenuation is controlled by the PARAM (EXT = 0x05) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 6: All options except for OCFG = 2 must be handled by the host via coefficient download in the CMXTBL command as explained in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 7: The decision to perform sampling rate conversion from 96KHz to 48KHz is done by comparing the output sampling rate specified via the SR parameter in the PLLCFG command to the input bitstream rate.

Note 8: When S/PDIF output is enabled (SPO = 1 in the CFG command), the ***AOUT3*** output is truncated to 16 bits.

12.2.4 MPEG

This command selects the MPEG stereo decoding function for MPEG-1 and MPEG-2, Layer II. Prior to calling this function, the host must load MPEG ADP microcode (refer to microcode release notes). The host can enable microphone mixing and/or 3D processing in this mode.

TABLE 101. MPEG Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00111b**				
parameter 1	PRLG		0000b				DMM	
parameter 2	SF	AB	BCFG		SW	OCFG		
parameter 3	CDLY			SRDLY				
parameter 4	00000000b							
parameter 5	00000000b							
parameter 6	00000000b							
parameter 7	PCMSF (m.s.)							
parameter 8	PCMSF (l.s.)							

TABLE 102. Parameter Description - MPEG

Parameter	Description	Values
PRLG	Dolby Pro Logic mode	(00b) No Pro Logic decoding (01b) Pro Logic decoding (10b) Reserved (11b) Reserved
DMM	dual mono reproduction mode	(00b) L channel to left output R channel to right output (01b) L channel to left and right outputs (10b) R channel to left and right outputs (11b) ((R + L) / 2) to left and right outputs
SF	Dolby Pro Logic surround filter (NR and LP filter)	(0) filters active (1) filters inactive
AB	auto balance (Dolby Pro Logic, only)	(0) effective (1) not effective
BCFG	bass redirection configuration	(00b) no bass redirection (01b) redirect to left and right (10b) reserved (11b) redirect to subwoofer
SW	sub-woofer output channel	(0) no subwoofer (1) subwoofer present

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Phone (408) 919-4111 Fax (408) 919-4122

TABLE 102. Parameter Description - MPEG

Parameter	Description	Values
OCFG	output speaker configuration	If PRLG = 0 or 3D is enabled, all values for OCFG result in 2/0 without down-mix. If PRLG = 1 and 3D is disabled, the following applies: (000b) 2/0 down-mix for Dolby Pro-Logic decoding (001b) 1/0 with center channel active (010b) 2/0 without down-mix (011b) 3/0 (100b) 2/1 (101b) 3/1 (110b) 2/2 (111b) 3/2
CDLY	center channel delay (0 - 5ms) in 1ms steps	(0 - 5) 0 - 5ms (0) for 3D
SRDLY	surround delay channel (0 - 15ms) in 1ms steps	(0 - 15) 0 - 15ms (without Dolby Pro Logic) (0 - 15) 15 - 30ms (with Dolby Pro Logic) (16) No delay (with Dolby Pro Logic) (16) 3D is enabled (without Dolby Pro Logic)
KAR	Karaoke mode	(0) disabled (1) enabled
RPC	maximum repeat count before muting	(0 - 7)
PCMSF (m.s)	output scale factor (most significant byte)	0x0000 min gain to 0x7FFF max gain
PCMSF (l.s.)	output scale factor (least significant byte)	

Note 1: If 3D is enabled (CDLY = 0 and SRDLY = 16), the output will always be 2/0 regardless of the OCFG value.

Note 2: If 3D is enabled, crossover will not be executed regardless of the BCFG value.

Note 3: The 3D setting can be changed during playback by a PARAM (EXT = 0x01) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 4: To enable microphone mixing, the host must write the PARAM (EXT = 0x06) ADP command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 5: Bass redirection attenuation is controlled by the PARAM (EXT = 0x05) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

12.2.5 DTS

This command selects the DTS S/PDIF output function. Prior to calling this function, the host must load DTS ADP microcode (refer to the microcode release notes). DTS decoding is not performed.

TABLE 103. DTS Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00100b**				
parameter 1	000b			SO	0000b			
parameter 2	00000000b							
parameter 3	00000000b							
parameter 4	00000000b							
parameter 5	00000000b							
parameter 6	00000000b							
parameter 7	00000000b							
parameter 8	00000000b							

TABLE 104. Parameter Description - DTS

Parameter	Description	Values
SO	serial port output	(0) S/PDIF output on ***S/PDIF*** pin. (1) S/PDIF output on ***AOUT[0]*** pin. The pin(s) on which S/PDIF is output is controlled by ADP microcode. Please refer to the microcode release notes in case the pin(s) are different than specified here.

12.2.6 PINK

This command instructs the ADP to generate pink noise. The host must load pink noise ADP microcode (refer to microcode release notes) to execute this function.

TABLE 105. PNG Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00011b**				
parameter 1	BCFG		000000b					
parameter 2	0	NS	L	C	R	LS	RS	SW
parameter 3	00000000b							
parameter 4	00000000b							
parameter 5	00000000b							
parameter 6	00000000b							
parameter 7	PCMSF (m.s.)							
parameter 8	PCMSF (l.s.)							

TABLE 106. Parameter Description - PINK

Parameter	Description	Values
BCFG	bass redirection configuration	(00b) no bass redirection (01b) redirect to left and right (10b) reserved (11b) redirect to subwoofer
NS	noise shaping filter	(0) on (1) off
L	left channel present flag	(0) no left channel (1) left channel present
C	center channel present flag	(0) no center channel (1) center channel present
R	right channel present flag	(0) no right channel (1) right channel present
LS	left surround channel present flag	(0) no left surround channel (1) left surround channel present
RS	right surround channel present flag	(0) no right surround channel (1) right surround channel present
SW	sub-woofer channel present flagl	(0) no subwoofer channel (1) subwoofer channel present
PCMSF (m.s)	output scale factor (most significant byte)	0x0000 min gain to 0x7FFF max gain
PCMSF (l.s.)	output scale factor (least significant byte)	

Note 1: Bass redirection attenuation is controlled by the PARAM (EXT = 0x05) command as shown in Section 12.4.1 “Special Function Parameter Command (PARAM)”.

Note 2: After downloading the pink noise generator microcode and issuing the CFG and PINK commands, the function is enabled by issuing a PLAY command. To stop the pink noise playback, a STOP command must be issued.

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12.3 Operation Control Commands

The commands in this group are PLAY, MUTE, UNMUTE, STOP, and STOPF.

12.3.1 Resume Operation (PLAY)

The PLAY command starts the operation of the selected function after a function selection command (PCM, AC3, MPEG), resumes operation of the selected function after a STOP command. It is required to activate this command after function selection command.

TABLE 107. PLAY Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01010b**				

12.3.2 Mute Operation (MUTE)

The MUTE command mutes the output (by inserting zeros) without stopping the operation of the selected function. This is a “hard” mute; It happens instantly without a “fade-out” period.

TABLE 108. MUTE Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01011b**				

12.3.3 Unmute Operation (UNMUTE)

The UNMUTE command restores the muted output while continuing the operation of the selected function. This is a “hard” unmute; It happens instantly without a “fade-in” period.

TABLE 109. UNMUTE Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01001b**				

12.3.4 Stop Operation (STOP)

Stops operation of the selected function by stopping the output and not requesting any more data. Data in the input buffer is preserved. Decoding will also stop after finishing to decode the current “half block” (128 samples).

TABLE 110. STOP Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01100b**				

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12.3.5 Stop Operation and Flush Buffers (STOPF)

The STOPF command stops operation of the selected function and mutes the output. Data in the ADP buffers is flushed out. After a STOPF command, decoding will start again after a function selection command, followed by a PLAY command.

TABLE 111. STOPF Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01101b**				

12.4 Set-up Commands

The commands in this group are: PARAM, CFG, SETIO, PLLTAB, PLLCFG and SPDIFCS. Please refer to IEC 958, Digital audio interface, 1989 for further details regarding the S/PDIF output format.

12.4.1 Special Function Parameter Command (PARAM)

This command allows the host to load special commands that extend the functionality of the application SW beyond the commands listed in Table 93 .

Each special command is specified by its EXT value and by a variable number of 24-bit data words. Each word is specified by 3 consecutive bytes, m.s. byte first. The number of data words is dependent on the value of EXT.

TABLE 112. PARAM Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10110b**				
parameter 1	EXT							
parameter 2	WORD 1 [23:16]							
parameter 3	WORD 1 [15:8]							
parameter 4	WORD 1 [7:0]							
parameter 5	WORD 2 [23:16]							
...	...							
parameter (N * 3) - 1	WORD N [23:16]							
parameter (N * 3)	WORD N [15:8]							
parameter (N * 3) + 1	WORD N [7:0]							

TABLE 113. Parameter Description - PARAM

Parameter	Description	Values
EXT	opcode extension	(0 - 255)
WORD i	data word value	variable

Ten such special commands have already been specified and implemented for the **ZR36710**. These commands are described below:

TABLE 114. Defined EXT functions

PARAM (EXT = 0x00) ADP Command - Volume Control	
PARAM (EXT = 0x00) (3-byte parameter)	Audio gain of left and right channels (gain affects both channels). WORD 1, bits [19:0]: 0x00000 = no gain. 0x7FFFF = maximum gain. All other bits are set to zero. The gain is treated as a 20.20 unsigned fraction. Note that the gain is reset to the value of the PCMSF parameter of the AC3, MPEG, PCM or LPCM commands whenever these commands are sent.

PARAM (EXT = 0x01) - Enable/Disable 3D processing (for AC3, PCM, LPCM and MPEG commands)	
PARAM (EXT = 0x01) (3-byte parameter)	Enable or disable the 3D processing for the AC3, PCM, LPCM and MPEG commands (2-channel mode only). WORD 1, bits [7:0]: 0x00 = disable 3D processing, 0x01 = enable 3D processing. All other bits are set to zero. The initial 3D setting is done by the SDRLY value in the AC3, PCM, LPCM or MPEG command. This PARAM command is used to change the 3D setting during playback. The setting of this PARAM command is overwritten by a following AC3, PCM LPCM or MPEG command.

PARAM (EXT = 0x02) - Audio/SCLK Tolerance	
PARAM (EXT = 0x02) (2-byte parameter)	Defines the tolerance allowed between the internal **SCLK** counter and the audio frame's DTS (provided in the bitstream) to maintain synchronization. If this difference falls outside the tolerance, then the next audio frame is either dropped or repeated. Measured in units of **SCLK** (90KHz). A value of 0 requires exact comparison.

PARAM (EXT = 0x03) - Audio Synchronization with SCLK	
PARAM (EXT = 0x03) (2-byte parameter)	0x0000 = Audio does not synchronize to **SCLK** counter. (no sync). 0x0001 = Audio synchronizes to **SCLK** counter (clock master mode). 0x0002 = **SCLK** synchronizes to timestamps in audio stream (audio master mode). 0x0003 = On next frame, audio syncs to **SCLK** (clock master) and then changes to audio master mode.

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Phone (408) 919-4111 Fax (408) 919-4122

PARAM (EXT = 0x04) - Karaoke Mode (for AC3 command)	
PARAM (EXT = 0x04) (21-byte parameter)	Controls the Karaoke mode for the AC3 command. WORD 1, bits [15:8]: Kl, default = 47 WORD 1, bits [7:0]: Ka, default = 47 WORD 2, bits [15:8]: Kb, default = 0 WORD 2, bits [7:0]: Kc, default = 33 WORD 3, bits [15:8]: Kd, default = 0 WORD 3, bits [7:0]: Ke, default = 0 WORD 4, bits [15:8]: Kf, default = 0 WORD 4, bits [7:0]: Kr, default = 47 WORD 5, bits [15:8]: Kg, default = 0 WORD 5, bits [7:0]: Kh, default = 47 WORD 6, bits [15:8]: Ki, default = 33 WORD 7, bits [23:0]: 0 All other bits are set to zero. The AC-3 output channels Lk, Ck and Rk are derived from encoded channels L, M, R, V1 and V2 as follows: Lk = Kl * L + Ka * V1 + Kb * V2 + Kc * M Ck = Kd * V1 + Ke * V2 + Kf * M Rk = Kr * R + Kg * V1 + Kh * V2 + Ki * M Requirements: Kl + Ka + Kb + Kc = 127 Kd + Ke + Kf = 127 Kr + Kg + Kh + Ki = 127

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

PARAM (EXT = 0x05) - Bass Redirection Attenuation (for AC3, PCM, LPCM, MPEG and PINK commands)	
PARAM (EXT = 0x05) (21-byte parameter)	Controls the Bass Redirection Attenuation for the AC3, PCM, LPCM, MPEG and PINK commands. WORD 1, bits [19:0]: A1, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 2, bits [19:0]: A2, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 3, bits [19:0]: A3, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 4, bits [19:0]: A4, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 5, bits [19:0]: A5, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 6, bits [19:0]: A6, default = 0x7FFFF, allowed values are 0x00000 (0) to 0x7FFFF (1.0) WORD 7, bits [19:0]: 0 All other bits are set to zero. The left channel output is multiplied by A1. The center channel output is multiplied by A2. The right channel output is multiplied by A3. The left surround channel output is multiplied by A4. The right surround channel output is multiplied by A5. The subwoofer channel output is multiplied by A6.

PARAM (EXT = 0x06) - Microphone Mixing Control (for AC3 and MPEG commands - 2-channel modes only)	
PARAM (EXT = 0x06) (3-byte parameter)	Controls the microphone mixing (input on ***AIN*** pin and ***AMCLK***, ***ALRCLK*** and ***ABCLK*** drive the ADC) for the AC3 and MPEG commands (2-channel modes only). WORD 1, bits [19:0]: MIC_SCALE, default = 0 All other bits are set to zero. MIC_SCALE is the scale factor for the microphone input, ranging from 0x00000 (0) to 0x7FFFF (1.0). Requirement: MIC_SCALE + PCMSF <= 1.0, PCMSF is taken from either the AC3, MPEG or PARAM (EXT = 0x00) commands. Microphone mixing performs the following: AOUT0_L = mic_input * MIC_SCALE + stream_output_L * PCMSF AOUT0_R = mic_input * MIC_SCALE + stream_output_R * PCMSF In which: AOUT0_L = left channel output AOUT0_R = right channel output stream_output_L = left decoded channel stream_output_R = right decoded channel mic_input = microphone input on ***AIN*** pin If S/PDIF output is encoded data, microphone mixing is not performed on the S/PDIF output. If S/PDIF output is PCM, microphone mixing is performed on the S/PDIF output.

ZORAN Corporation 3112 Scott Blvd., Santa Clara, CA 95054
Phone (408) 919-4111 Fax (408) 919-4122

PARAM (EXT = 0x06) - Voice Extractor Mode Control (for PCM command)	
PARAM (EXT = 0x06) (9-byte parameter)	Controls the Voice Extractor mode and microphone scale setting for the PCM command. WORD 1, bits [19:0]: MIC_SCALE, default = 0, maximum = 0x7FFFF. WORD 2, bits [19:0]: MUSIC_SCALE, default = 0, maximum = 0x7FFFF. WORD 3, bits [19:0]: VOICE_SCALE, default = 0, maximum = 0x7FFFF. All other bits are set to zero. MIC_SCALE is the scale factor for the microphone input. Requirement: MIC_SCALE + MUSIC_SCALE + VOICE_SCALE <= 0x7FFFF.

PARAM (EXT = 0x06) - Size of Custom Channel Downmix Table (for LPCM command)	
PARAM (EXT = 0x06) (3-byte parameter)	Size of the downmix table (in bytes) that gets loaded by PARAM (EXT = 0x07). WORD 1, bits [19:0]: Size. All other bits are set to zero. This command is optional. If this command is not issued, the default size is 222 bytes. This command should only be entered if the downmix table is sparse, thus reducing the amount of data to transfer.

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PARAM (EXT = 0x07) - CMXTBL (Custom Channel Downmix Table for LPCM command)

PARAM
(EXT = 0x07)
(222-byte parameter)

Custom channel downmix table. If the downmix table is not 222 bytes, then PARAM (EXT = 0x06) must be issued prior to this command.

WORD 1, bits [23:0]: ACTIVE_OUTPUTS. See below for definition.

WORD 2, bits [23:0]: OUT_CHAN_INC0. See below for definition.

...

WORD 10, bits [23:0]: OUT_CHAN_INC8. See below for definition.

WORD 11, bits [19:0]: K_00. 20-bit coefficient, right-justified.

...

WORD 74, bits [19:0]: K_77. 20-bit coefficient, right justified.

All other bits are 0.

ACTIVE_OUTPUTS: The number of output channels after downmix. Default is 2.

OUT_CHAN_INCj: The distance (in words) to advance the ADP output buffer pointer before placing the next sample into the output buffer. If there are n active output channels, then n+1 of these entries are meaningful; values for n+2 to 8 will be ignored. The sum of the n+1 entries will be 8 to ensure that the next sample will start at a distance of 8 words from the start of where the last sample was stored.

The function is as follows:

AOUT0_L		K00	K01	K02	K03	K04	K05	K06	K07		ACH0
AOUT0_R		K10	K11	K12	K13	K14	K15	K16	K17		ACH1
AOUT1_L		K20	K21	K22	K23	K24	K25	K26	K27		ACH2
AOUT1_R		K30	K31	K32	K33	K34	K35	K36	K37		ACH3
AOUT2_L	=	K40	K41	K42	K43	K44	K45	K46	K47	*	ACH4
AOUT2_R		K50	K51	K52	K53	K54	K55	K56	K57		ACH5
AOUT3_L		K60	K61	K62	K63	K64	K65	K66	K67		ACH6
AOUT3_R		K70	K71	K72	K73	K74	K75	K76	K77		ACH7

or:

AOUT0_L = K00*ACH0+K01*ACH1+K02*ACH2+K03*ACH3+K04*ACH4+K05*ACH5+K06*ACH6+K07*ACH7

AOUT0_R = K10*ACH0+K11*ACH1+K12*ACH2+K13*ACH3+K14*ACH4+K15*ACH5+K16*ACH6+K17*ACH7

etc.

Output channels: AOUT0_L, AOUT0_R, AOUT1_L, AOUT1_R, AOUT2_L, AOUT2_R, AOUT3_L, AOUT3_R.

Input channels: ACH0, ACH1, ACH2, ACH3, ACH4, ACH5, ACH6, ACH7.

Mixing coefficients: K00, ..., K77 in which:

-1.0 = 0x80000
0.0 = 0x00000
1.0 = 0x7FFFF
default: K00 = K11 = 0x7FFFF, all other values are 0.

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12.4.2 Serial Ports Configuration (CFG)

The CFG set-up command determines the audio input and output configurations for the **ZR36710**.

TABLE 115. CFG Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00010b**				
parameter 1	11000000b							
parameter 2	00011000b							
parameter 3	CPB	CPA	FRB			FRA		
parameter 4	000b			ERR	00b		ISP	OSP
parameter 5	00b		SPO	INW		OUTW		0
parameter 6	00000000b							
parameter 7	SPBS							
parameter 8	00b		FMB			FMA		

TABLE 116. Parameter Description - CFG

Parameter	Description	Values
CPB	Serial clock B polarity. Selects which edge (negative or positive) of ***ABCLK*** that ***AOUT*** and ***ALRCLK*** are sampled on. Must be the same value as CPA.	(0) negative (1) positive
CPA	Serial clock A polarity. Selects which edge (negative or positive) of ***ABCLK*** that ***AIN*** is sampled on. Must be the same value as CPB.	(0) negative (1) positive
FRB	Frame size (bits) of group B serial ports (output). Indicates the number of ***ABCLK*** cycles during each level of ***ALRCLK*** (1/2 period). For S/PDIF output the value 001b should be used. Must be the same value as FRA.	(000b) 16 (001b) 32 (also for S/PDIF) (111b) 24
FRA	Frame size (bits) of group A serial ports (input). Indicates the number of ***ABCLK*** cycles during each level of ***ALRCLK*** (1/2/ period). Must be the same value as FRB.	(000b) 16 (001b) 32 (111b) 24
ERR	Error output pin enable. Currently asserted by AC-3 decoder errors. One block decode period duration.	(0) disabled (1) GPAIO[1] is configured as error output
ISP	Input word select polarity. Selects which polarities of ***ALRCLK*** determine the left and right channels on ***AIN***.	(0) left channel corresponds to ***ALRCLK*** low (1) left channel corresponds to ***ALRCLK*** high
OSP	Output word select polarity. Selects which polarities of ***ALRCLK*** determine the left and right channels on ***AOUT***.	(0) left channel corresponds to ***ALRCLK*** low (1) left channel corresponds to ***ALRCLK*** high
SPO	S/PDIF output. Designates the ***S/PDIF*** pin as either a S/PDIF transmitter or a fourth reconstructed stereo output ***AOUT[3]***.	(0) ***AOUT[3]*** - must be 0 in AC-3 6-channel mode. (1) ***S/PDIF***

TABLE 116. Parameter Description - CFG

Parameter	Description	Values
INW	Input serial port word size. Selects the size of the word on ***AIN***.	(00b) 20 bits (01b) 18 bits (10b) 16 bits (11b) 24 bits
OUTW	Output serial port word size. Selects the size of the word on ***AOUT***.	(00b) 20 bits (01b) 18 bits (10b) 16 bits (11b) 24 bits
SPBS	Group B internal clock divider.	See Table 29 in Section 4.6 on page 72.
FMB	Serial ports group B format. Selects the positioning of ***AOUT*** in relation to ***ALRCLK***.	(000b) left justified (001b) left justified+1 bit (***ABCLK*** cycle) (111b) right justified
FMA	Serial ports group A format. Selects the positioning of ***AIN*** in relation to ***ALRCLK***.	(000b) left justified (001b) left justified+1 bit (***ABCLK*** cycle) (111b) right justified

The CFG command must be followed by an AC3, MPEG, PCM, LPCM or PINK function selection command.

12.4.3 PLL Table (PLLTAB)

The PLLTAB command defines the PLL programmable registers.

The audio master clock is used to generate the output serial port clocks. The audio master clock (***AMCLK***) frequency is generated by the PLL as follows:

$$f(GCLK1) \times \frac{AUDM}{AUDD} = f(AMCLK)$$

The processing clock (***PCLK***) is generated by the PLL as follows:

$$f(GCLK) \times \frac{DSPM}{DSPD} = f(PCLK)$$

Note that the value of AUDD is limited to:

$$\frac{f(GCLK1)}{AUDD} > 8KHz$$

The value of DSPD is limited to:

$$\frac{f(GCLK)}{DSPD} > 1MHz$$

TABLE 117. PLLTAB Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**11000b**				
parameter 1	SR			AUDD (bits 12 - 8)				
parameter 2	AUDD (bits 7 - 0)							
parameter 3	000b			AUDM (bits 12 - 8)				
parameter 4	AUDM (bits 7 - 0)							
parameter 5	00b		DSPD					
parameter 6	DSPM							

TABLE 118. Parameter Description - PLLTAB

Parameter	Description	Values
SR	output sampling rate	(000b) 48 KHz (001b) 44.1 KHz (010b) 32 KHz (011b) 96 KHz for PCM
AUDM	13-bit multiplier for ***AMCLK*** generation	see equations above
AUDD	13-bit divider for ***AMCLK*** generation	limited according to the equations above
DSPM	8-bit multiplier for ***PCLK*** generation	see equations above
DSPD	6-bit divider for ***PCLK*** generation	limited according to the equations above

12.4.4 PLL Configuration(PLLCFG)

The PLLCFG command defines the PLL configuration. This command must be entered before the CFG command. The command responds with one byte status (PLLR as explained below).

TABLE 119. PLLCFG Command/Status Structure

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
opcode	**1**	**0**	**0**	**11001b**				
parameter 1	SR			000b			AS	DS
status 1 (PLLR)	000000b						PA	PD

Note: A delay of 50 microseconds is required after any change of the AS and DS fields of the PLLCFG command before entering another ADP command.

TABLE 120. Parameter /Status Description - PLLCFG

Parameter	Description	Values
SR	output sampling rate	(000b) 48 KHz (001b) 44.1 KHz (010b) 32 KHz (011b) 96 KHz for PCM (111b) the sampling rate is specified in the bitstream
AS	audio PLL set	(0) no action (1) resets ***AMCLK*** PLL
DS	process PLL set	(0) no action (1) resets ***PCLK*** PLL
PA (PLLR)	***AMCLK*** lock indication	(0) not locked (1) locked
PD (PLLR)	***PCLK*** lock indication	(0) not locked (1) locked

Notes:

- SR = 111b should be used only if the sampling rate is not known beforehand as the locking delay may be up to 50 msec. This delay has to be taken into account by the decoding function SW.
- Upon power-up of the **ZR36710**, the ADP internal SW (microcode) sets DSPM to 3 and DSPD to 1 and locks the ***PCLK*** section of the PLL. The host should not start communication with the **ZR36710** before it receives an indication that the ***PCLK*** section is locked by the setting of the **PLLpLOCKED** ISR bit in the **ZR36710**.

The PLLR reply is a one-byte response to the PLLCFG command. The byte indicates the status of PLL sections: PA = 1, ***AMCLK*** is locked. PD = 1, ***PCLK*** is locked.

12.4.5 S/PDIF (SPDIFCS)

The SPDIFCS command enables the S/PDIF output and provide channel status information to be inserted in the S/PDIF output signal.

TABLE 121. SPDIFCS Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10101b**				
parameter 1	0000b				channel status (27:24)			
parameter 2	channel status (15:8)							
parameter 3	channel status (7:0)							
parameter 4	00000000b							

TABLE 122. Parameter Description - SPDIFCS

Bit(s)	Description	Values
27 - 24	Sampling rate	(0x0) 44.1KHz (0x2) 48KHz (0x3) 32KHz
15 - 8	Category code	defined in IEC 958 specification
7, 6	Mode	(0) Mode 0
5 - 3	de-emphasis mode	(000b) no de-emphasis (001b) 15/50 de-emphasis
2	copyright indication	(0) digital copy prohibited (1) digital copy permitted
1	data mode. Selects the type of data output on the ***S/PDIF*** pin when it is configured as a S/PDIF transmitter (SPO = 1).	(0) PCM data. Must be 0 if SPO = 0. (1) non-PCM encoded data
0	usage mode	(0) consumer

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12.4.6 Set/Test the Programmable I/O Pins (SETIO)

The SETIO command returns the current value of the GPIOC and GPIO registers (SETIOR1 and SETIOR2 respectively) and then changes their values.

The GPIOC parameter bits, enabled by the GPIOC_MASK bits, are copied to the least significant two bits of the GPIOC register.

The GPIO parameter bits, enabled by the GPIO_MASK bits, are copied to the GPIO register.

The GPIOC register selects the direction of the GPIO pins (0 for input and 1 for output).

The GPIO register selects the signal level of the GPIO pins that were selected as output (0 for low level and 1 for high level).

In the **ZR36710**, only the two l.s. bits affect the two ***GPAI/O*** pins of the **ZR36710**. The other four bits are reserved and should be masked.

TABLE 123. SETIO Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10010b**				
parameter 1	00b		GPIOC_MASK					
parameter 2	00b		GPIOC					
parameter 3	00b		GPIO_MASK					
parameter 4	00b		GPIO					

TABLE 124. Parameter Description - SETIO

Parameter	Description	Values
GPIOC_MASK	1 in bit i means: update GPIOC register bit i according the value in the next field in bit i	
GPIOC	The value to be copied to bit i of the GPIOC register if GPIOC_MASK is equal to 1 in this bit	
GPIO_MASK	1 in bit i means: update GPIO register bit i according the value in the next field in bit i	
GPIO	The value to be copied to bit i of the GPIO register if GPIO_MASK is equal to 1 in this bit	

The SETIOR reply is a 2-byte response to the SETIO command. The first byte (SETIOR1) is the value of the GPIOC register before the change. The second byte (SETIOR2) is the value of the GPIO register before the change.

TABLE 125. SETIOR1 and SETIOR2 Status Structure

	7	6	5	4	3	2	1	0
status 1 (SETIOR1)	00b		GPIOC					
status 2 (SETIOR2)	00b		GPIO					

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12.5 Microcode Loading and Debug Commands

The microcode loading and debug commands are BOOT, INTRP, POKE, PEEK and VER.

12.5.1 Load Program (BOOT)

The BOOT command loads a new ADP microcode program (specified by the parameter bytes of the command) to the ADP RAM. The data format is described below. After the program has been loaded, the execution is transferred to the address specified in the boot data stream.

TABLE 126. BOOT Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10000b**				
parameter 1								
...	...							
parameter Z								

The boot program may contain several “packets” stored sequentially. Each packet is prefaced by a header consisting of three 32-bit words:

- RAM target address - address where the program packet has to be loaded or the execution start address.
- Number of code words (N) to be loaded.
- Block repeat count (M).

Starting from the word #4, there are N 32-bit program words to be loaded.

Each of the three header words are interpreted as 20-bit right-justified words (the most significant 12 bits of the 32-bit word are ignored).

There are 3 packet types distinguished by N:

- If N > 0, the N 32-bit data words are copied to RAM at the target address specified in the header. The byte ordering for these words within the boot ROM is m.s. byte first. During the copying stage, each word is repeated M times.
- If N = 0, the target address is interpreted as an execution start address. In this case, the processor will jump to the execution start address after all packets have been loaded. If more than one packet contains an execution address, the last one will be used. If no execution address is specified, the processor will jump to a fixed address in the ROM “command dispatcher” routine.
- If N = 0xFFFFF, it indicates that this packet is the last packet, the loading process is stopped and the program is continued from the execution start address (as mentioned above).

M = 1 if no repeat is needed. A block repeat count of 0 will repeat each word 1048576 times.

12.5.2 Interpret an Instruction (INTRP)

The INTRP command builds a 32-bit word from the four bytes following the opcode and executes it as an ADP instruction.

TABLE 127. INTRP Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10001b**				
parameter 1	instruction (bits 31:24)							
parameter 2	instruction (bits 23:16)							
parameter 3	instruction (bits 15:8)							
parameter 4	instruction (bits 7:0)							

12.5.3 Load Memory Data (POKE)

The POKE command writes a data block of **size** (parameters 4 to 7) elements (of 4 bytes each) to the ADP RAM, starting at **address** (parameters 1 to 3).

TABLE 128. POKE Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10011b**				
parameters 1 - 3	address (bits 23:0)							
parameters 4 - 7	size (bits 31:0)							
parameter 8	data[1] (bits (31:24)							
parameter 8 + 4 * size	data[size] (bits 7:0)							

12.5.4 Return Memory Data (PEEK)

The PEEK command returns a data block of **size** (parameters 4 to 7) elements (of 4 bytes each) from the ADP RAM, starting from **address** (parameters 1 to 3).

TABLE 129. PEEK Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10100b**				
parameters 1 - 3	address (bits 23:0)							
parameters 4 - 7	size (bits 31:0)							

12.5.5 ROM Version Code (VER)

The VER command returns (by sending four READ commands) the four bytes (m.s. byte first) of the ADP ROM version number (VERR).

TABLE 130. VER Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**00001b**				

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12.6 Status Request Commands

The only status request command is STAT.

12.6.1 Return Status Information (STAT)

The STAT command allows bytes of status information to be returned by sending READ commands following the STAT command.

TABLE 131. STAT Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**01110b**				

The ADP returns the status of the operation in progress and information about the decoded bitstream. Some of the status fields are common for all functions. The number and contents of the other status fields are function-specific as described below for AC3, PCM, LPCM, MPEG and DTS.

The different responses can be recognized by the 5 l.s. bits of the first status byte which are the same as the 5 l.s. bits of the opcode byte that selected the current function.

The first response byte, before the status byte, is the number of status bytes. The last response byte, after the all the status bytes is the ISTATUS byte explained in Section 12.1 “ADP Command Overview”.

12.6.2 AC-3 Status Reply (AC3STATR)

This reply is a response to the STAT command when the AC3 function is selected.

TABLE 132. AC3STATR Status Structure

	7	6	5	4	3	2	1	0
status 1	STATUS			00101b				
status 2	RST		AC3DST			AC3IST		
status 3	00000000b							
status 4	00000000b							
status 5	DIFT (m.s.)							
status 6	DIFT (l.s.)							
status 7	SR		IDR					EW
status 8	0000b				EF	CCFG		
status 9	BSID					BSM		
status 10	CM		SM		DS		C	OR
status 11	000b			DN2				
status 12	000b			DN				
status 13	LC2							
status 14	LC							
status 15	P2	RT2		ML2				
status 16	P	RT		ML				

Status Fields:

- STATUS - Global status of operation in progress:

  000b = No errors.

  001b = Updated status information is not yet available (a new command has been received and is being processed).

  010b = Operation error. AC3DST and AC3IST further explain the type of error.

- RST - Run status:

  00b = running.

  01b = stopped.

- AC3DST - Status returned by AC-3 decode routine:

  000b = No errors.

  001b = Input error status is non-zero and last output block was repeated.

  010b = Input error status is non-zero and outputs were muted.

  011b = Unsupported bitstream identification revision.

  100b = Unsupported number of channels in input stream.

- AC3IST - Status returned by AC-3 Frame Information routine:

  000b = No errors.

  001b = Invalid frame sync.

  010b = Invalid sample rate.

  011b = Invalid coded data bit rate.

- DIFT - A/V synchronization status. It represents a signed difference between PTS and **SCLK**. If the difference is larger than maximum representable number (approximately 0.35 sec), it will be set to the maximum value.
- SR - Sampling rate:

  00b = 48 KHz.

  01b = 44.1 KHz.

  10b = 32 KHz.

- IDR - Coded data bit rate in units of Kbits/Sec:

  32 (00000b), 40 (00001b), 48 (00010b), 56 (00011b), 64 (00100b), 80 (00101b), 96 (00110b), 112 (00111b), 128 (01000b), 160 (01001b), 192 (01010b), 224 (01011b), 256 (01100b), 320 (01101b), 384 (01110b), 448 (01111b), 512 (10000b), 576 (10001b), 640 (10010b).

- EW - Extra word present in coded frame:

  0 = Not present or not applicable.

  1 = Present. Applicable only for 44.1KHz.

- CCFG - Coding mode:

  000b = Dual mono.

  001b = 1/0, front center only.

  010b = 2/0, front left and right.

  011b = 3/0, front left, right and center.

  100b = 2/1, front left, front right and surround.

  101b = 3/1, front left, right and center and surround.

  110b = 2/2, front left and right and surround left and right.

  111b = 3/2, front left, right and center and surround left and right.

- BSID - Bitstream identification number.
- BSM - Bitstream mode:

  000b = Main audio service.

  001b = Main audio service minus dialogue.

  010b = Associated service for the visually impaired.

  011b = Associated service for the hearing impaired.

  100b = Associated service, dialogue.

  101b = Associated service, commentary.

  110b = Associated service, emergency flash.

- CM - Center mix:
  - 00b = -3 db.
  - 01b = -4.5 db.
  - 10b = -6 db.
- SM - Surround mix:
  - 00b = -3 db.
  - 01b = -6 db.
  - 10b = None.
- DS - Dolby surround mode:
  - 00b = No indication.
  - 01b = Not Dolby surround encoding.
  - 10b = Dolby surround encoded.
- C - Copyright protection:
  - 0 = Not protected.
  - 1 = Protected.
- OR - Original/Copy indication:
  - 0 = Copy.
  - 1 = Original.
- DN2 - Dialogue normalization for channel 2 in dual mono mode (CCFG = 000b).
- DN - Dialogue normalization for normal operation.
- LC2 - Language code for dual mono mode (CCFG = 000b).
- LC - Language code for normal operation.
- P2 - Production information for channel 2 in dual mono mode (CCFG = 000b):
  - 0 = Does not exist.
  - 1 = Exists.
- RT2 - Room type for channel 2 in dual mono mode (CCFG = 000b):
  - 00b = No indication.
  - 01b = Large room.
  - 10b = Small room.
- ML - Mix level value for channel 2 in dual mono mode (CCFG = 000b).
- P - Production information for normal operation:
  - 0 = Does not exist.
  - 1 = Exists.
- RT - Room type for normal operation:
  - 00b = No indication.
  - 01b = Large room.
  - 10b = Small room.

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Phone (408) 919-4111 Fax (408) 919-4122

- ML - Mix level value for normal operation.

12.6.3 PCM Status Reply (PCMSTATR)

This reply is a response to the STAT command when the PCM function is selected.

TABLE 133. PCMSTATR Status Structure

	7	6	5	4	3	2	1	0
status 1	STATUS			00110b				
status 2	RST	000000b						
status 3	00000000b							
status 4	00000000b							
status 5	00000000b							
status 6	00000000b							
status 7	VERSION							
status 8	00000000b							

Status Fields:

- STATUS and RST have the same meaning as for AC3STATR.
- VERSION - PCM ROM SW version number.

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12.6.4 LPCM Status Reply (LPCMSTATR)

This reply is a response to the STAT command when the LPCM function is selected.

TABLE 134. PCMSTATR (8-channel) Status Structure

	7	6	5	4	3	2	1	0
status 1	STATUS			00100b				
status 2	RST		00000b					BFS
status 3	00000010b							
status 4	00000000b							
status 5	DIFT (m.s.)							
status 6	DIFT (l.s.)							
status 7	E	M	0	AFN				
status 8	QWL		SR		0	NAC		

Status Fields:

- STATUS - Global status of operation in progress:
  - 000b = No errors.
  - 001b = Operation error.
- RST and DIFT have the same meaning as for AC3STATR.
- BFS - Buffer status:
  - 0 = No underflow.
  - 1 = Underflow.
- E - Emphasis flag:
  - 0 = No emphasis.
  - 1 = Emphasis.
- M - Mute flag:
  - 0 = No mute.
  - 1 = Mute.
- AFN - Audio frame number.
- QWL - Quantization word length:
  - 00b = 16 bits.
  - 01b = 20 bits.
  - 10b = 24 bits.
  - 11b = Reserved.
- SR - Sampling frequency:
  - 0 = 48 KHz.
  - 1 = 96 KHz.

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- NAC - Number of audio channels:

  0 = 1 channel.

  1 = 2 channels.

  ...

  7 = 8 channels.

12.6.5 MPEG Status Reply (MPEGSTATR)

This reply is a response to the STAT command when the MPEG function is selected.

TABLE 135. MPEGSTATR Status Structure

	7	6	5	4	3	2	1	0
status 1	STATUS			00111b				
status 2	RST		000b			MPGST		
status 3	00000000b							
status 4	00000000b							
status 5	DIFT (m.s.)							
status 6	DIFT (l.s.)							
status 7	0000b				ID	LAY		PRT
status 8	BR				SFR		PAD	PRV
status 9	MODE		MEXT		CPR	ORG	EMPH	
status 10	00000000b							
status 11	00000000b							
status 12	00000000b							

Status Fields:

- STATUS, RST and DIFT have the same meaning as for AC3STATR.
- MPGST - Status returned by MPEG-1 decode routine:

  000b = No errors.

  001b = Invalid frame sync.

  010b = CRC error.

  011b = Invalid sample rate.

  100b = Invalid data rate.

The next 20 bits copy the 20 bits of the MPEG-1 audio frame header which follow the sync word (ISO 11172-3 Sections 2.4.1.3 and 2.4.2.3)

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Phone (408) 919-4111 Fax (408) 919-4122

- ID - Algorithm ID:
  - 0 = Reserved.
  - 1 = MPEG.
- LAY - Layer:
  - 00b = Reserved.
  - 01b = Reserved.
  - 10b = Layer II.
  - 11b = Reserved.
- PRT - Protection bit:
  - 0 = CRC word is present.
  - 1 = No CRC word.
- BR - Bit-rate index (see second table in Section 2.4.2.3 in ISO 11172-3).
- SFR - Sampling frequency:
  - 00b = 44.1 KHz.
  - 01b = 48 KHz.
  - 10b = 32 KHz.
  - 11b = Reserved.
- PAD - Padding bit:
  - 0 = The frame does not contain an additional “slot”.
  - 1 = The frame contains an additional “slot” (1 byte for layer II).
- PRV - Private bit, value has no meaning for MPEG audio decoding.
- MODE - Encoding mode:
  - 00b = Stereo.
  - 01b = Joint-stereo.
  - 10b = Dual channel.
  - 11b = Single channel.
- MEXT - Mode extension (see ISO 11172-3 Section 2.4.2.3).
- CPR - Copyright protection:
  - 0 = Not copyright protected.
  - 1 = Copyright protected.
- ORG - Original/Copy:
  - 0 = Copy.
  - 1 = Original.
- EMPH - Emphasis:
  - 00b = None.
  - 01b = 50/15us.
  - 10b = Reserved.
  - 11b = CCITT J.17.

12.6.6 DTS Status Reply (DTSSTATR)

This reply is a response to the STAT command when the DTS function is selected.

TABLE 136. DTSSTATR Status Structure

	7	6	5	4	3	2	1	0
status 1	STATUS			00100b				
status 2	RST		000b			DTSST		
status 3	00000000b							
status 4	00000000b							
status 5	DIFT (m.s.)							
status 6	DIFT (l.s.)							
status 7	00000b					BR		
status 8 - 12	00000000b							

Status Fields:

- STATUS - Global status of operation in progress:
  - 000b = No errors.
  - 001b = Status information is not yet available.
  - 010b = Operation error.
  - 011b - 111b = reserved.
- RST and DIFT have the same meaning as for AC3STATR.
- DTSST - Frame information status:
  - 000b = No error.
  - 001b = Invalid frame sync.
  - 010b - 011b = reserved.
  - 100b = Invalid.
  - 101b = Input underflow.
  - 110b - 111b = reserved.
- BR - Bit rate:
  - 000b = reserved.
  - 001b = 188.250 kbps.
  - 010b = 251.250 kbps.
  - 011b = 377.250 kbps.
  - 100b = 503.250 kbps.
  - 101b = 754.500 kbps.
  - 110b = 1509.750 kbps.
  - 111b = reserved.

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13. Annex B: Pin Assignment and Signal Status

13.1 Pin assignment

Following is the pin assignment list. When a pin has two alternative functions both names appear. Note that some of the pins has a third or even a fourth function for testing purposes. These additional functions are not listed here.

TABLE 137. Pin Assignment: Pins 1 - 80

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	*GND*	21	*HD[0]*	41	*GND*	61	*RAMDQM*
2	*GPSI*	22	*HA[3]*	42	*RAMADD[5]*	62	*RAMDAT[8]*
3	*HD[15]*	23	*GND*	43	*RAMADD[2]*	63	*VDD*
4	*HD[14]* *CDFRM*	24	*HA[2]*	44	*RAMADD[6]*	64	*RAMDAT[7]*
5	*HD[13]* *CDDAT*	25	*HA[1]*	45	*RAMADD[1]*	65	*RAMDAT[9]*
6	*HD[12]* *CDCLK*	26	*HA[0]*	46	*RAMADD[7]*	66	*RAMDAT[6]*
7	*HD[11]*	27	*HWR#* *WR/W#*	47	*RAMADD[0]*	67	*RAMDAT[10]*
8	*VDD*	28	*VDD*	48	*VDD*	68	*GND*
9	*HD[10]*	29	*HCS#*	49	*RAMADD[8]*	69	*RAMDAT[5]*
10	*HD[9]*	30	*HRD#* *HDS#*	50	*RAMADD[10]*	70	*RAMDAT[11]*
11	*HD[8]*	31	*HRDY*	51	*RAMADD[9]*	71	*RAMDAT[4]*
12	*HD[7]*	32	*HACK#*	52	*RAMADD[11]*	72	*RAMDAT[12]*
13	*GND*	33	*VDD*	53	*GND*	73	*VDD*
14	*HD[6]*	34	*HIRQ#*	54	*RAMCS#[0]*	74	*RAMDAT[3]*
15	*HD[5]*	35	*HWID*	55	*RAMCS#[1]*	75	*RAMDAT[13]*
16	*HD[4]*	36	*HORD*	56	*RAMRAS#*	76	*RAMDAT[2]*
17	*HD[3]*	37	*HTYPE*	57	*PCLK*	77	*RAMDAT[14]*
18	*VDD*	38	*RAMADD[4]*	58	*VDD*	78	*RAMDAT[1]*
19	*HD[2]*	39	*RAMADD[3]*	59	*RAMCAS#*	79	*RAMDAT[15]*
20	*HD[1]*	40	*GND*	60	*RAMWE#*	80	*GND*

TABLE 138. Pin Assignment: Pins 81 - 160

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
81	*GND*	101	*Y[0]*	121	*GND*	141	*RESET#*
82	*RAMDAT[0]*	102	*C[7]*	122	*GPAI/O[0]*	142	*IDLE*
83	*TESTMODE*	103	*VDD*	123	*GPAI/O[1]*	143	
84	*VCLK*	104	*C[6]*	124	*VCLKx2*	144	*DVDSOS*
85	*VMASTER*	105	*C[5]*	125	*GND*	145	*GND*
86	*VDD*	106	*C[4]* *OSDPLT*	126	*GCLK1*	146	*DVDVALID*
87	*VDEN#*	107	*C[3]* *OSDPEL[3]*	127	*SCNENBL*	147	*DVDSTRB*
88	*CBLANK*	108	*GND*	128	*XO*	148	*DVDREQ*
89	*VSYNC*	109	*C[2]* *OSDPEL[2]*	129	*GCLK*	149	*DVDDAT[0]*
90	*HSYNC*	110	*C[1]* *OSDPEL[1]*	130	*STNDBY*	150	*VDD*
91	*FI*	111	*C[0]* *OSDPEL[0]*	131	*GND*	151	*DVDDAT[1]*
92	*Y[7]*	112	*AIN*	132	*AMCLK*	152	*DVDDAT[2]*
93	*GND*	113	*VDD*	133	*VDD*	153	*DVDDAT[3]*
94	*Y[6]*	114	*AOUT[0]*	134	*PLLGND*	154	*DVDDAT[4]*
95	*Y[5]*	115	*AOUT[1]*	135	*PLLCFG[0]*	155	*VDD*
96	*Y[4]*	116	*AOUT[2]*	136	*PLLCA*	156	*DVDDAT[5]*
97	*Y[3]*	117	*S/PDIF* *AOUT[3]*	137	*PLLCFG[1]*	157	*DVDDAT[6]*
98	*VDD*	118	*ALRCLK*	138	*PLLVDD*	158	*DVDDAT[7]*
99	*Y[2]*	119	*ABCLK*	139	*ICEMODE*	159	*GPSO*
100	*Y[1]*	120	*GND*	140	*VDD*	160	*GND*

13.2 Signal status during RESET and STNDBY

In Table 139 , the status of the pins during and just after RESET and during STANDBY are described. The **ZR36710** has an automatic power-up reset process that is initiated if the voltage slope lasts less than 10 mSec. In order to ascertain proper reset under any conditions, it is suggested that a proper reset process will be initiated using the ***RESET#*** signal after power-up or at other times that a reset process is needed, e.g. to change level on one of the input pins that are allowed to change only during RESET. In a proper reset process, the ***RESET#*** signal has to be activated for at least 160 ***GCLK*** periods.

the RESET period starts 16 ***GCLK*** periods after activation of the ***RESET#*** signal and ends 16 ***GCLK*** periods after de-activation of the ***RESET#*** signal. 128 ***GCLK*** periods after activation of the ***RESET#***

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Phone (408) 919-4111 Fax (408) 919-4122

signal, the PLL reverts to the default multiplication and division factors (1/1 for ***PCLK***, 1/4 for ***AMCLK***).

The ***STNDBY*** signal should be activated only during RESET. It should be activated at least 160 ***GCLK*** periods after activation of the ***RESET#*** signal and de-activated at least 32 GCLK periods before de-activation of the ***RESET#*** signal. When ***STNDBY#*** and ***RESET#*** are held asserted together, all outputs and bidirectional pins float, such that the **ZR36710** is electrically disconnected from its surroundings. All internal clocks are disabled, and power consumption is minimized.

During RESET or STNDBY some of the signals are internally pulled up (p.u.) or pulled down (p.d.).

The following notes apply to this table:

1. During RESET, this signal's direction (output with unknown level, or input) is determined by the level on the ***VMASTER*** input signal.
2. During RESET, this signal's status (output or 3-S) is determined by the level on the ***VDEN#*** input signal.
3. During RESET or just after RESET, all output signals which are not pulled and for which no specific level appear in the table, the value is unknown.
4. During RESET, the values of these outputs indicate the NOP SDRAM command. Shortly after RESET, a pre-charge command is output once and then again a (repeated) NOP command.
5. During or just after RESET, the ***PCLK*** output is the clock signal at the current rate set by the PLL operation.
6. The host should not access the **ZR36710** during RESET. Then it should poll the **PLLpLOCKED** status bit.

TABLE 139. Signal Status during RESET and STANDBY

Pin Name	RESET	STNDBY	Note
GPSI	input	input	
HD[15:0]	input (p.d.)	3-S (p.d.)	
HA[3:0]	input	input	
HWR#	input	input	
HCS#	input	input	6
HRD#	input	input	
HRDY	output (low)	3-S	
HACK#	output (high)	3-S (p.u.)	
HIRQ#	3-S (p.u.)	3-S (p.u.)	
HWID	input	input	
HORD	input	input	
HTYPE	input	input	
RAMADD[11:0]	output	3-S	3

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Phone (408) 919-4111 Fax (408) 919-4122

Pin Name	RESET	STNDBY	Note
RAMCS#[1:0]	output	3-S (p.u.)	4
RAMRAS#	output	3-S (p.u.)	4
PCLK	output	3-S	5
RAMCAS#	output	3-S (p.u.)	4
RAMWE#	output	3-S (p.u.)	4
RAMDQM	output	3-S (p.u.)	3
RAMDAT[15:0]	input (p.d.)	3-S (p.d.)	
TESTMODE	input	input	
VCLK		3-S (p.d.)	1
VMASTER	input	input	
VDEN#	input	input	
CBLANK	output	3-S (p.d.)	3
VSYNC		3-S (p.d.)	1
HSYNC		3-S (p.d.)	1
FI		3-S (p.d.)	1
Y[7:0]		3-S (p.d.)	2
C[7]		3-S (p.d.)	2
AIN	input	input	
AOUT[3:0]	output (low)	3-S	
ALRCLK	output (low)	3-S	
ABCLK	output (low)	3-S	
GPAI/O[1:0]	input	3-S	
VCLKx2		3-S	1
GCLK1	input	input	
SCNENBL	input	input	
GCLK	input	input	
STNDBY	input	input	
AMCLK	input	3-S	
PLLCFG[1:0]	input	input	
ICEMODE	input	input	
RESET#	input	input	
IDLE	output (high)	3-S (p.u.)	
DVDSOS	input	input	
DVDVALID	input	input	
DVDSTRB	input	input	
DVDREQ	output (low)	3-S	
DVDDAT[7:0]	input	input	
GPSO	output (low)	3-S	

14. Annex C: Programming Sequence for Playback

This section explains the proper sequence of loading set-up parameters and microcode to the **ZR36710** in order to playback DVD VOB bitstreams. Information is given in later sub-sections on how to playback other types of bitstreams and if any extra information is required (e.g. microcode release notes or application notes) beyond the information provided in this data sheet for their support.

14.1 Stage 1: PLL Initialization and Stabilization

After power-up, the host activates the ***RESET#*** pin for at least 160 ***GCLK*** cycles. The host must wait until V_{DD}, ***GCLK*** and ***RESET#*** are stable for at least 30 milliseconds before activation of ***RESET#***.

The first stage of initializing the **ZR36710** after RESET is to select and stabilize the frequencies of ***PCLK*** and ***AMCLK***. These values are derived from the frequencies on the ***GCLK*** and ***GCLK1*** pins, respectively. As explained in Section 4.2 “Phase-Locked Loop Interface”, the following configuration is recommended:

- **ZR36710** operates in video sync-master mode: ***GCLK*** = ***GCLK1*** = 27 MHz.
- **ZR36710** operates in video sync-slave mode: ***GCLK*** = ***GCLK1*** = ***VCLKx2*** = 27 MHz.

By using the recommended frequencies of 27 MHz for ***GCLK*** and ***GCLK1***, the default values of *DSPM, DSPD, AUDM* and *AUDD* (PLLTAB and PLLCFG ADP commands) will stabilize ***PCLK*** and ***AMCLK*** to 81 MHz and 256 x 48 KHz respectively, without requiring the host to load these parameters.

Deactivation of the ***RESET#*** pin activates the ***IDLE*** pin and starts the PLL locking process explained in Section 4.2 “Phase-Locked Loop Interface”. While the device is attempting to lock it’s PLL values after RESET, the following holds true:

- **C-STATE** = 00 0000b (***reset*** state) in the **STATUS0** register.

Since several audio bitstreams with different audio sampling rates can be played, the ***AMCLK*** value can be re-initialized several times after power-up so it is not so important to stabilize ***AMCLK*** at power-up. However, ***PCLK*** is only initialized once at power-up and can not be changed unless another ***RESET#*** signal is applied.

If ***GCLK*** is not equal to 27 MHz, then the default values of *DSPM* and *DSPD* can not be used to generate ***PCLK*** and these values must be changed. If the host must change *DSPM* and *DSPD*, then the host calls the PLLTAB and PLLCFG ADP commands to change the *DSPM* and *DSPD* values to guarantee ***PCLK*** = 81 MHz.

The **ZR36710** will indicate to the host that ***PCLK*** has been locked by two means:

- **PLLpLOCKED** = 1 in the ISR.
- **C-STATE** = 00 0010b (***init_pclk*** state) in the **STATUS0** register.

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Phone (408) 919-4111 Fax (408) 919-4122

Once ***PCLK*** is stabilized, then the initialization process of the device can proceed to the next stage explained below.

14.2 Stage 2: I/O Port Configuration

Once ***PCLK*** is stabilized, the SDRAM, coded bitstream port, video and audio ports must be configured.

14.2.1 SDRAM, Host Bus Port and Coded Bitstream Port Configuration

The SDRAM and coded bitstream ports are configured by loading the following general set-up parameters as explained in Sections 4.1 “SDRAM Interface” and 4.4 “DVD-DSP and CD-DSP Interfaces”. The host bus port is configured by pins except for one aspect: whether or not ***HACK#*** is used in Type B transfers, which is configured by loading the following set-up parameters. These ports can only be initialized once after RESET. If these ports need to be re-initialized, then another RESET must be executed before new values are loaded:

- *SysConfig*: Selects the number of 16Mbit SDRAM devices used, selects whether or not ***HACK#*** is used in Type B transfers, enables/disables the decryption circuitry, selects the coded bitstream source and the burst size of the coded data transfers.
- *SDConfig*: Configures the DVD-DSP and/or CD-DSP interfaces.

14.2.2 Audio Port Configuration

The audio port is configured by loading the following ADP commands as explained in Sections 4.2 “Phase-Locked Loop Interface” and 4.6 “Audio Interface”. The audio port can only be configured once after RESET. If this port needs to be re-initialized, then another RESET must be executed before new values are loaded:

- CFG and SPDIFCS ADP commands: Configures the audio port signals.
- *AUDM* and *AUDD* (PLLTAB and PLLCFG ADP commands): Configures the ratios for the four supported sampling rates.

14.2.3 Video Port Configuration

The video port is configured by loading the following general set-up parameters as explained in Section 4.5 “Video Interface”:

- *VidConfig*: Configures the sync and clock polarities, pixel bus width, enables/disables SAV and EAV sync code insertion, enables/disables pixel value limiting and selects the OSD source.
- *ColorV*, *ColorY*, *ColorU*: Background color.
- *VidOut*: Indicates to the DVP the display frame rate (NTSC or PAL) and field polarity.
- *Htotal*, *Vtotal*: Number of pixels and lines per display frame, respectively.
- *HSyncSize*, *VSyncSize*: Size of horizontal and vertical blanking regions, respectively.
- *ActiveStartX*, *ActiveEndX*, *ActiveSizeX*: Configures the active horizontal pixel region.
- *ActiveStartY*, *ActiveEndY*, *ActiveSizeY*: Configures the active vertical line region.
- *CaptionOffset*: Sets the line in which closed caption data is placed.

If a composite blanking signal is required by a video encoder or some other device in the system, then the following parameters should be loaded at this time. If the ***CBLANK*** output is used by the system for other purposes such as a tri-state enable for PIP applications as explained in Section 4.5.7 “Disabling the Video Output and PIP Applications”, these parameters can be loaded after this stage as needed.

- *CBHStart*, *CBVStart*, *CBHEnd*, *CBVEnd*: Configures the waveform of the ***CBLANK*** output.

The video processing unit (VPU) does not make use of these values until a write to the *StartDisplay* set-up parameter is executed. Once this parameter is written, the video port begins to generate output signals based on the values of the parameters. Also, the state of the device changes as follows:

- **C-STATE** = 00 0011b (***init_display*** state) in the **STATUS0** register.

The host can change the values of the video port parameters (e.g. changing from NTSC output to PAL output) without having to execute a RESET. To change the video port parameters more than once after RESET, the following must occur:

- **C-STATE** = 00 0011b (***init_display***) or 11 0000b (***Idle***) in the **STATUS0** register.
- New video port parameters are loaded.
- The *StartDisplay* parameter is re-loaded so the **ZR36710** will operate with the new video port values.

Once all the ports are configured, the device is ready for decoding preparation as explained below.

14.3 Stage 3: OSD Display and Preparation for Decoding

Once the **ZR36710** is in either the ***init_display*** or ***Idle*** states as indicated by the **C-STATE** bits of the **STATUS0** register, the device is configured for playback of a particular type of bitstream. In addition to

preparation for playback, OSD display can also be executed at this time. Unless otherwise specified, the following parameters can only be changed while the device is in the ***init_display*** or ***Idle*** states.

14.3.1 OSD Display

Once the video port is enabled, the OSD features of the **ZR36710** can be enabled. OSD is either provided externally by the OSD port pins or provided internally by writing OSD data to the OSD Data Register. The following general set-up parameters must be loaded to make use of the OSD. These parameters are explained further in Section 9. “On-Screen Display”:

- *OSDControl*: Configures the OSD plane configuration, pixel width, and plane-switching mechanism.
- *OSDPalette0i* (0 <= *i* <= 15): Configures palette 0 and blending for each of the 16 pixel values.
- *OSDPalette1i* (1 <= *i* <= 15): Configures palette 1 and blending for each of the 16 pixel values.
- *OSDMemStart*: Starting byte address within OSD buffer to begin using pixel data.
- *OSDMemSize*: Number of bytes within the OSD buffer of pixel data to use.
- *OSDFirstLine*: First line in the active video area to begin displaying OSD data.
- *OSDLastLine*: Last line in the active video area to display OSD data.
- *OSDSwitch*: Enables/Disables OSD display.

The buffer in the OSD region of the SDRAM can be loaded with OSD data in the format described in Section 9. “On-Screen Display”. The default size of this buffer is 52KB. This data is written via the OSD Address Register and OSD Data Register as explained in the aforementioned section. The set-up parameters explained above must be loaded prior to OSD display.

The OSD data can be changed at any time after the video port is enabled, whether the device is in the ***Idle*** state or not. Care should be taken by the system to ensure that OSD data is not changed while it is being displayed or else temporary artifacts may appear on the screen due to the change in the OSD data. The system should also ensure that an address written to the OSD Address Register is within the range of the OSD buffer in the SDRAM.

14.3.2 Microcode Loading - DVP and ADP

Whether or not OSD is used, the first step in preparing the **ZR36710** for playback is to load the appropriate DVP and ADP microcodes.

The DVP microcode is loaded via writing to a general set-up parameter address as explained in Section 5.1.3 “Loading Microcode via the General Set-up Parameters”. The maximum size of the microcode is 12288 bytes. This microcode is mandatory for playback with the device; Without this microcode, the **ZR36710** cannot playback any bitstream. If the host loads a DVP microcode and then needs to load a different DVP microcode prior to issuing a **start** host command, then the host needs to zero-pad the original DVP microcode to 16384 bytes before loading the replacement microcode.

For some applications, up to four init files have to be loaded to parameter address 0xF0 to 0xF3, together with the microcode files. See Section 5.1.3 “Loading Microcode via the General Set-up Parameters”. In

the case of Init file #3 that gets written to parameter address 0xF2, it can only be loaded once after each time the **ZR36710** is taken out of RESET.

The ADP microcode is loaded via sending the BOOT ADP command as explained in Section 12.5.1 “Load Program (BOOT)”. The maximum size of this microcode is 12288 bytes. To take advantage of special features of the ADP (e.g. 3D audio algorithms, Karaoke mixing, etc.), the appropriate ADP microcode must be loaded at this time.

14.3.3 Bitstream, Disc and Entry Point Selection

Once the microcode is loaded, the following general set-up parameters must be loaded which select the type of disc to be read (DVD or CD) and the type of bitstream that will be parsed and/or decoded. The microcode loaded to the DVP must be applicable to the settings of these parameters:

- *DiscType*: Selects the type of disc (DVD or CD) if the bitstream is not provided across the host bus. Also selects the DVD sector size if bitstream is provided on the DVD-DSP interface.
- *BitstreamSelect*: The *CBSelect* bits select the type of bitstream to be parsed and/or decoded.

The video entry point within the video stream from which decoding begins is also selected by the following parameter:

- *BitstreamSelect*: The *VidEntry* bit determines which headers within the video bitstream the DVP will parse to and start decoding at once the **start** host command is issued.

14.3.4 Stream ID Selection and Audio Sampling Rate Selection

The audio, video and sub-picture stream IDs of the desired content to decode should be selected prior to decoding by writing the appropriate values to the following general set-up parameters:

- *AudSID*: Selects audio stream (or sub-stream) ID.
- *VidSID*: Selects video stream ID.
- *SPSID*: Selects sub-picture sub-stream ID.

The video and sub-picture stream IDs can be changed during playback (**C-STATE** is not equal to ***Idle***), allowing changing on the fly. Audio stream ID can be changed during playback as explained in Section 14.5 “Also For: Changing Audio Parameters During Playback”.

The audio sampling rate is selected by writing the following ADP command:

- *SR* (PLLCFG ADP command): Selects the audio sampling rate.

Once the audio sampling rate is selected, the device will lock ***AMCLK*** to the associated sampling frequency. The **ZR36710** will indicate that the audio portion of the PLL is locked by:

- **PLLaLOCKED** = 1 in the ISR.

14.3.5 A/V Synchronization Parameters - Delays and Tolerances

The following parameters indicate whether or not the video and/or audio will synchronize to the **SCLK** counter within the device. These parameters may be changed at any time during playback (**C-STATE** is not equal to ***Idle***), disabling and re-enabling synchronization on the fly:

- *VidSyncMode*: The *VsyncMode* bit enables/disables video sync to **SCLK**.
- PARAM (EXT = 0x03) ADP command: This ADP command enables/disables audio sync to **SCLK**.

The PARAM (EXT = 0x03) ADP command is also responsible for selecting “clock master” or “audio master” synchronization, determining if **SCLK** is a free-running clock or if it is synchronized to the audio time stamps as explained in Section 6.10 “A/V Synchronization”.

The following general set-up parameters indicate an offset added to the video and/or audio DTS/PTS values to compensate for reconstruction chain delays for both the video and audio. This is further explained in Section 6.10 “A/V Synchronization”:

- *VidPortDelay*: Indicates the added delay to the video DTS for synchronization purposes.
- *AudPortDelay*: Indicates the added delay to the audio PTS for synchronization purposes.

The following parameters indicate the tolerances allowed between the video DTS and **SCLK** and/or the audio PTS and **SCLK** before a frame is either paused or skipped as explained in Section 6.10 “A/V Synchronization”. These parameters can be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing flexible tolerances on the fly:

- *VidTolerance*: Defines the tolerance between the video DTS and **SCLK** before repeating/skipping frames.
- PARAM (EXT = 0x02) ADP command: Defines the tolerance between the audio PTS and **SCLK** before freezing/skipping audio frame output (clock master mode only).

14.3.6 Initializing Sub-picture and Closed Captions

The following general set-up parameters initialize the sub-picture mechanism of the **ZR36710** in case sub-picture data is decoded and displayed. These parameters may be switched at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically change the settings of the sub-picture decoder:

- *SPPalette*: Loads the sub-picture palette into the **ZR36710**.
- *SPSwitch*: Determines which sub-picture DCSQ’s trigger the display of sub-pictures.

The following general set-up parameters initialize the closed caption decoder. These parameters may be switched at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically change the settings of the closed caption decoder:

- *CaptionWord*: Defines the closed caption data to be inserted if no closed caption information is found in the bitstream or if playback is paused.
- *CaptionSwitch*: Enables/Disables closed captions insertion.

14.3.7 Display Aspect Ratio, Zoom and NTSC <-> PAL Conversion Parameters

The following parameters define if aspect ratio conversion and/or panning of a picture is handled automatically by the **ZR36710**. These parameters may be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing dynamic switching of how the scaling is handled within the device, either automatically by the **ZR36710** or by general set-up parameters loaded to the device, and also allowing either the panning to be handled by the device automatically or by general set-up parameters loaded to the device:

- *DVPGen2*: Selects the source aspect ratio of the decoded image.
- *AutoScaling*: Enables/Disables automatic aspect ratio conversion within the **ZR36710**.
- *AutoPanScan*: Enables/Disables automatic picture panning within the **ZR36710**.

If automatic aspect ratio conversion and/or automatic panning is disabled, then the following general set-up parameters are loaded by the host to define which decoded pixels will be scaled. These parameters can be changed while decoding takes place (**C-STATE** is not equal to ***Pause*** or ***Idle***), allowing the host to dynamically change the window of decoded pixels to be scaled:

- *PanScanBaseX*, *PanScanSizeX*, *PanScanOffsetX*, *PicSizeX*, *DynPanX*: Defines the horizontal region of decoded pixels to be used by the scaler.
- *PanScanBaseY*, *PanScanSizeY*, *PanScanOffsetY*, *PicSizeY*, *DynPanY*: Defines the vertical region of decoded pixels to be used by the scaler.

If automatic aspect ratio conversion and/or automatic panning is disabled, then the following general set-up parameter is loaded by the host to define the horizontal and vertical scaling ratios. This parameter may be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically change the scaling ratios per picture, including any zooming effects:

- *ScaleRatio*: Selects the horizontal and vertical scaling ratios to apply to the decoded image.

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If automatic aspect ratio conversion is disabled, then the following general set-up parameters are loaded by the host to define the image area on the display in which the scaled video is placed. These parameters should coordinate with the *PanScan* and *ScaleRatio* parameters. These parameters can be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically change the image area:

- *ImageStartX*, *ImageEndX*, *ImageSizeX*: Defines the horizontal image coordinates.
- *ImageStartY*, *ImageEndY*, *ImageSizeY*: Defines the vertical image coordinates.

The following general set-up parameter defines the scaling ratio for the sub-picture display in the case of NTSC <-> PAL conversion. This parameter may be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically scale the sub-picture display:

- *SPScale*: Defines the scaling ratio for the sub-picture display. Does not scale the sub-picture positioning, however.

14.3.8 Audio Volume and Mute Control

The following ADP commands define the audio gain and muting status. These commands may be issued at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically change the volume of the audio and mute/unmute the audio:

- PARAM (EXT = 0x00) ADP command: Sets the volume.
- MUTE or UNMUTE ADP command: Mutes/unmutes the audio.

14.3.9 Miscellaneous Pixel Bus Control

The following general set-up parameters determine when background color is displayed instead of the decoded image:

- *PlaybackMode*: The *LastPic* bit determines whether or not background is displayed in place of the decoded image after decoding is complete and the device returns to the ***Idle*** state. The *Black* bit determines whether or not the background color is forced to black while a decoded image is displayed in the image region.
- *BackgroundSwitch*: Enables/Disables forcing of the background color in place of the decoded image on the display. This parameter can be changed at any time during playback (**C-STATE** is not equal to ***Idle***), allowing the host to dynamically force the background color on and off on the display.

The following general set-up parameter allows tri-stating of the video port:

- *PlaybackMode*: The *VidFloat* bit determines whether or not to float the video port of the **ZR36710**. If this bit is used to float the video port, only a RESET will take the video port out of high-impedance.

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14.4 Decoding/Playback

If encrypted VOB files are to be played from a DVD, both disc key and title key transfer must be performed with the **ZR36710** prior to any attempt at playback. In a PC environment where data is retrieved from a DVD-ROM drive, an authentication procedure must be executed prior to any key transfer. The details of this procedure are provided in a separate application note to CSS licensed developers as explained in Section 6.2 “DVD Authentication and Decryption”. If decryption is to be bypassed and the DVD-DSP interface is used for bitstream transfer, the following parameter must be provided:

- *PlaybackMode*: The *DVDReqEnable* bit determines whether or not to disable the ***DVDREQ*** signal. This signal only needs to be disabled during a special mode of operation during the title key transfer process of the decryption as explained in a separate application note.

Before starting the playback process, the interrupt from the **ZR36710** to the host must be configured to allow for ***VSYNC*** interrupts. For example, this can be done by:

- Clearing the **VSYNC** bit in the IMR (IMR = 0xDFFF).

The host has the option of disabling all interrupt sources except ***VSYNC*** and still allow playback to be handled correctly without missing any important information due to disabled interrupts. Operating in this manner is a suggestion only, not a requirement. Even though only ***VSYNC*** will enable interrupts to the host, on each interrupt the host should check all the bits of the ISR in case one of the following holds true:

- A NV_PCK has been parsed out of the bitstream and is ready for the host to read.
- The DVP output buffer (DVPO_FIFO) is full, ready for host retrieval.
- A code buffer became full/empty.

Playback begins with the host issuing a **start** host command to the Host Command Register. The **HCREADY** bit in the **STATUS1** register indicates when a host command may be issued to the device. At this time:

- The **ZR36710** deactivates the ***IDLE*** signal. **IDLE** = 0 in the **STATUS1** register.
- **C-STATE** = 10 0000b (***Nspb*** - active video) or 10 1000b (***Nspb*** - no video) in the **STATUS0** register.

Bitstream transfer begins through the DVD-DSP interface or host bus (or CD-DSP interface for CD streams). If the host bus is used for the coded bitstream transfer, the host must either monitor the ***HRDY*** pin or **HRDY** bit in the **STATUS1** register to make sure that the coded data FIFO does not overflow, or the host bus must be configured to wait on ***HACK#*** to trigger as explained in Section 4.3.5 “Coded Data Request for Host Bus Code Transfers - HRDY”. If the DVD-DSP interface is used for bitstream transfer, the **ZR36710** will request bitstream via the ***DVDREQ*** signal.

The **ZR36710** will automatically initialize **SCLK** to the first SCR encountered within the bitstream and **SCLK** will increment at 90KHz. If the synchronization scheme is audio master, **SCLK** is updated by the ADP as necessary. The host has the option of reinitializing **SCLK** to the next SCR encountered within the bitstream (assuming no SCR discontinuities are in the bitstream). This is done by writing to the following parameter:

- *VidSyncMode*: Setting *Vlock* initializes **SCLK** to the first SCR encountered.

The video data will be discarded by the DVP until the correct entry point has been found (according to the *VidEntry* bit in the *BitstreamSelect* parameter). Once the correct entry point into the bitstream is found, the code buffers within the SDRAM are filled with data.

Decoding begins on the next ***VSYNC*** once **SCLK** matches the video DTS of the first frame in the video code buffer and the field polarity of the first frame to decode is correctly matched with the display field polarity. Presentation of video, audio and sub-picture data is according to the set-up parameters entered as explained in Section 14.3 “Stage 3: OSD Display and Preparation for Decoding” and Section 6. “Video, Audio and Sub-picture Decoding”.

On every ***VSYNC***, an interrupt is generated to the host. It is at this time that the host should check the **DVPOBF** bit of the ISR to see if new frame information is ready in the DVP output buffer. Since a new frame begins decoding on ***VSYNC*** boundaries, it is important for the host to retrieve this data on each ***VSYNC*** that new data is available or risk having the data overwritten by new frame data. If the host has no need for this data, then the host can ignore this status bit.

On each ***VSYNC*** interrupt the host should check if the **NAVREADY** bit of the ISR is set, indicating that a new NV_PCK has been extracted and is ready to be read through the NAV Address and NAV Data Registers. It is important for the host to retrieve this information for HLI support.

In case **NAVREADY** = 1, the host checks the **DVP_SW[0]** and **NAVBUF** bits of the **STATUS1** register to see which segment of the NAV buffer in the SDRAM contains the relevant data. Once the segment of the NAV buffer is known, then the retrieval of the data via the NAV Address and NAV Data Registers takes place.

The host must extract the HLI information from the retrieved NV_PCK and write it back to the following general set-up parameters:

- *HiLightButton1*: Button 1 coordinate information and color table selection.
- *HiLightButton2*: Button 2 coordinate information and color table selection.
- *HiLightColor1*: Color information table 1 for HLI buttons.
- *HiLightColor2*: Color information table 2 for HLI buttons.
- *HiLightColor3*: Color information table 3 for HLI buttons.
- *HiLightTiming*: Timing information for HLI buttons.
- *HiLightSwitch*: Display instructions for HLI buttons.

As explained in Section 6.11 “Host Commands and Control over the Playback Operation”, the host can send host commands to the Host Command Register to pause playback, single step and other various

functions. The host must check if **HCREADY** = 1 in the **STATUS1** register before sending each host command.

The playback will end on either of the following conditions:

- An appropriate end code was encountered within the bitstream.
- The **end_playback** host command was issued by the host.

In either case, the **ZR36710** will activate the ***IDLE*** signal and return to the ***Idle*** state. If an end code is encountered within the bitstream, either the last frame displayed is frozen on the output or the background color is displayed as specified by the *LastPic* bit of the *PlaybackMode* set-up parameter. If playback is stopped by an **end_playback** host command, the 'E' parameter in this host command determines whether the background color is displayed or the last decoded frame is frozen on the output.

Once the **ZR36710** is in the ***Idle*** state, changes can be made to the video port parameters as explained in Section 14.2 "Stage 2: I/O Port Configuration". Also, all parameters and microcode outlined in Section 14.3 "Stage 3: OSD Display and Preparation for Decoding" can be changed at this time.

Once the host issues another **start** host command, the playback process is repeated.

14.5 Also For: Changing Audio Parameters During Playback

The following sections explain how the audio stream ID and/or audio parameters are changed during playback of DVD, VideoCD and CD-DA data.

14.5.1 Making the Change for DVD and VideoCD

The following sequence of operations is required to change the audio stream ID and/or parameters during playback of DVD or VideoCD:

- Set *AudSID* = 0x00FF and wait 50 milliseconds.
- Download the appropriate microcode for the new audio standard using the BOOT ADP command and wait 1 millisecond.
- Send the CFG ADP command and wait 1 millisecond.
- Send the SPDIFCS ADP command and wait 1 millisecond.
- Send the appropriate ADP function command (e.g. AC3 command).
- Set the audio synchronization with the PARAM (EXT = 0x03) ADP command.
- Send the PLAY ADP command.
- Set *AudSID* to an active value (e.g. 0x0080).

Note 1: When changing *AudSID* without changing the audio standard (i.e.. changing from AC-3 to LPCM is changing the audio standard, whereas changing between two AC-3 stream IDs is not changing the audio standard), do not execute the 2nd, 3rd and 4th steps.

Note 2: When changing one (or more) parameters of the CFG command without changing the audio standard, do not execute the 2nd step.

Note 3: When changing one (or more) parameters of the SPDIFCS ADP command without changing the audio standard, do not execute the 2nd and 3rd steps.

Note 4: When changing one (or more) parameters of the SPDIFCS ADP command while changing the audio standard, do not execute the 3rd step.

Note 5: When using "audio master" synchronization mode, send a parameter value of 0x03 in step 6.

14.5.2 Making the Change for CD-DA

The following sequence of operations is required to change the audio parameters during playback of CD-DA:

- Send the **end_playback** host command.
- Send the CFG ADP command and wait 1 millisecond.
- Send the SPDIFCS ADP command and wait 1 millisecond.
- Send the appropriate PCM ADP command.
- Send the **start** host command.

Note 1: The 2nd step is required only to change a parameter in the CFG ADP command. If no parameter is changed in the CFG ADP command, do not execute the 2nd step.

Note 2: When changing a parameter in the PCM ADP command without changing any parameter in the CFG and SPDIFCS ADP commands, do not execute the 2nd and 3rd steps.

14.6 Also For: VideoCD or CD-I (FMV) Streams

If the bitstream is an MPEG-1 system stream embedded within VideoCD or CD-I (FMV) sectors (*CBSelect* = 00000b), during all modes of operation (especially for trick modes such as fast search and random access), the host will inform the **ZR36710** which sectors to play and the **ZR36710** will, in turn, inform the host to temporarily pause reading from the disk and inform the host when to resume reading valid bitstream from the disc and from which sector. The following is the sequence of operations:

- Wait for **IDLE** in the **STATUS1** register to be set. This can be achieved by issuing an **end_playback** command or by resetting the **ZR36710**.
- Determine which sectors to play by writing the start and end sector addresses to the DVP input FIFO as explained in Section 5.6.1 "Writing Data to the DVP Data Register". The format of the data written to the FIFO is shown in Table 140 .

TABLE 140. Start and End Sector Addresses written to DVP Input FIFO

	15 - 8	7 - 0
Type	0x0001	
parameter 1	start sector address - minutes[a]	start sector address - seconds[a]
parameter 2	00000000b	start sector address - sectors[a]
parameter 3	end sector address - minutes[a]	end sector address - seconds[a]
parameter 4	00000000b	end sector address - sectors[a]
parameter 5	0x0000	
...	0x0000	
parameter 31	0x0000	
Note : In order to have a start sector address but have no end sector address, the host should write 0x9999 to parameter 3 and 0x0099 to parameter 4.		

a. in binary-coded decimal format

- Send the **start** host command.
- Start feeding bitstream via the CD-DSP interface. The **ZR36710** will discard sectors until the start sector address is encountered.
- Wait until an interrupt arrives from the **ZR36710**. If the interrupt source is **DVPOBF**, the host must read the data in the DVPO_FIFO as explained in Section 5.6.2 “Reading Data from the DVP Data Register”. The data may be one of two new data types, PAUSE_DRIVE and RESUME_DRIVE, defined in Table 141 and Table 142 .

TABLE 141. PAUSE_DRIVE request in DVPO_FIFO

	15 - 14	13 - 8	7	6 - 0
Tag Word	01b	0000010b		0000001b
parameter 1	minutes		seconds	
parameter 2	00000000b		sectors	

TABLE 142. RESUME_DRIVE request in DVPO_FIFO

	15 - 14	13 - 8	7	6 - 0
Tag Word	01b	0000000b		0000010b

- If the PAUSE_DRIVE request is read, the host should pause the CD-DSP device from sending valid data. The “minutes”, “seconds” and “sectors” values (each in binary-coded decimal format) indicate the sector address that was last processed so the host knows at which sector address to resume when requested to do so.
- If the RESUME_DRIVE request is read, the host should instruct the CD-DSP device to resume sending valid data. The starting sector address at which data transfer resumes must be before the last processed sector as indicated by the PAUSE_DRIVE request.

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- Once the end sector address is reached, the **ZR36710** waits until all available pictures are decoded and displayed and then goes into the ***Idle*** state.

14.7 Also For: Random Access for Special VideoCD Streams

The host may request the **ZR36710** to start playback from the nearest I-picture, GOP or sequence header. There are many special VideoCD streams in which the sequence header appears only once (at the beginning of the clip). If the **ZR36710** detects an I-picture during random access, the information which resides in the sequence header (e.g. quantization tables) may be needed for proper display.

In this case, the host should first send the bitstream at the beginning of the clip that includes the sequence header information. After sending this information, the bitstream transfer resumes from the middle of the VideoCD clip. The following sequence of operations explains how to transfer the sequence header information without displaying the first picture of the clip.

- Wait for **IDLE** in the **STATUS1** register to be set. This can be achieved by issuing an **end_playback** command or by resetting the **ZR36710**.
- Download the VideoCD DVP microcode (if it is not already loaded).
- Instruct the **ZR36710** to process the sequence header only. This is done by setting bit 0 of *DVPGen2* as shown in Table 143 .

TABLE 143. Processing sequence header in VideoCD via *DVPGen2* bit 0

***DVPGen2* (0x04)**	
15 - 1	**0**
*	Seqhdr
* = Bits used for other functions that must be left as they were.	
Seqhdr	0 = Process all pictures in a VideoCD bitstream. 1 = Process only the sequence header in a VideoCD bitstream.

- Send the **start** host command.
- Send the bitstream from the beginning of the clip/file to the **ZR36710**.
- Wait for **IDLE** in the **STATUS1** register to be set. The **ZR36710** processes the sequence header and GOP. The **ZR36710** goes into the ***Idle*** state once it reaches the first picture after the GOP.
- Instruct the **ZR36710** to process all pictures in a VideoCD bitstream by clearing bit 0 of *DVPGen2* as shown in Table 143 .
- Send the **start** host command.
- Send the bitstream to the **ZR36710** from a random position in the VideoCD clip as explained in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”.

14.8 Also For: MPEG-1 System Streams

If the bitstream is an MPEG-1 system stream (*CBSelect* = 00111b), the following applies:

- The **NAVREADY** bit of the ISR will not be set since no NV_PCK information will be provided in an MPEG-1 system stream.
- The sub-picture decoder is disabled since sub-picture data does not exist in MPEG-1 system streams.
- The **DRAMBF** and **SPCBF** bits of the **STATUS0** register are irrelevant.
- The **NAVBUF**, **HLI_TIME** and **SPDERR** bits of the **STATUS1** register are irrelevant.
- The end of the bitstream is encountered when the DVP parses an ISO_11172_end_code.

14.9 Also For: CD-DA Sectors

If the bitstream is PCM audio data provided via CD-DA sectors (*CBSelect* = 00100b), the following applies:

- A/V sync is disabled since no video exists within the bitstream The ADP begins output of the PCM data as it receives it.
- The **NAVREADY** bit of the ISR will not be set since no NV_PCK information will be provided in a PCM audio stream.
- CD-DA playback via the CD-DSP interface is explained in greater detail in a separate application note. Issues the application note concentrates on is how the **ZR36710** handles a bitstream provided at a constant bit rate, how the **ZR36710** provides sector addresses as mentioned in Section 5.6 “Writing and Reading the DVP Data Register - Reg. 0x6” and others.
- The sub-picture decoder is disabled since sub-picture data does not exist in PCM audio streams.
- Only the **ACBE** and **ACBF** bits of the **STATUS0** register are relevant regarding buffer full/empty indication. **DRAMBF**, **VCBE**, **VCBF** and **SPCBF** are irrelevant.
- **C-STATE** can only have the following values: 10 1000b or 01 1000b during playback.
- The **NAVBUF**, **PICTYPE**, **FRAME/FIELD#**, **HLI_TIME** and **SPDERR** bits of the **STATUS1** register are irrelevant.
- The end of the bitstream is met only when the **end_playback** host command is issued.

14.10 Also For: VideoCD Auxiliary Data Sectors (block decoding)

If the bitstream is VideoCD auxiliary data sectors (*CBSelect* = 00101b), the function of the **ZR36710** becomes performing block decoding, extracting the relevant data and providing it to the host. The following steps are done to achieve this:

- The **NAVREADY** bit of the ISR may be ignored since no NV_PCK data will be provided. Block decoding ADP microcode and VideoCD DVP microcode are required for this task.
- Send the **start** host command, but do not begin data transfer to the **ZR36710**.
- Send the block decoding ADP command in the format shown in Table 144 .

TABLE 144. Block Decoding (PARAM w/EXT = 5) Command Structure

	7	6	5	4	3	2	1	0
opcode	**1**	**0**	**0**	**10110b**				
parameter 1 (EXT)	00000101b							
parameter 2	StartSectorMin							
parameter 3	StartSectorSec							
parameter 4	StartSectorNum							
parameter 5	00000000b							
parameter 6	NumOfSectors							
parameter 7	Mode							

TABLE 145. Parameter Description - Block Decoding

Parameter	Description	Values
StartSectorMin, StartSectorSec, StartSectorNum	3 bytes containing the address of the first sector that should be processed. The sector address should be specified as it appears in the sector header. Sectors with lower addresses will be ignored.	2 BCD digits for StartSectorMin 2 BCD digits for StartSectorSec 2 BCD digits for StartSectorNum (BCD = binary coded decima).
NumOfSectors	Number of sectors to process (starting from the first processed sector).	1 to 64
Mode	Type of sectors (CD-ROM or VideoCD)	(0x10) Mode 1 (CD-ROM) (0x21) Mode 2 Form 1 (VideoCD)

- Once the block decoding ADP command has been sent, bitstream transfer can begin (e.g. across the CD-DSP interface).
- The host sends the STAT ADP command to monitor the progress of the operation. The result of this command is in the following structure:

TABLE 146. Block Decoding Status Structure

	7	6	5	4	3	2	1	0
status 1	FinishedFlag							
status 2	NumSectors							
status 3	ErrorCode							
status 4	00000000b							
status 5	SectorError0							
...	...							
status 12	SectorError7							

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Phone (408) 919-4111 Fax (408) 919-4122

Status Fields:

FinishedFlag - Indicates the process is finished. Once finished, the host can read the data from the NAV buffer (up to 64 2KByte sectors). All other status fields are not valid until the process is finished:

0 = Not finished.

1 = Finished.

NumSectors - Number of sectors written to SDRAM.

ErrorCode - Indicates a fatal error condition that terminates the process. In such a case, not all of the sectors indicatd by NumSectors are processed:

0 = No error.

2 = The first wrong sector was mode 0.

3 = The first wrong sector was mode 1, different from the requested mode.

4 = The first wrong sector was mode 2 form 1, different from the requested mode.

5 = The first wrong sector was mode 2 form 2.

6 = The first wrong sector address was not in order.

7 = The first wrong sector's first 12 bytes are not a SYNC pattern.

8 = Timeout due to missing data.

SectorError0 - Each bit indicates the EDC for each processed sector. The l.s. bit indicates the EDC for sector 0. The m.s. bit indicates the EDC for sector 7. Bad EDC does not cause a fatal error and does not terminate the process. For each bit:

0 = Good EDC.

1 = Bad EDC.

SectorError*n* - Each bit indicates the EDC for each processed sector. The l.s. bit indicates the EDC for sector (n * 8). The m.s. bit indicates the EDC for sector ((n+1) * 8 - 1). Bad EDC does not cause a fatal error and does not terminate the process. For each bit:

0 = Good EDC.

1 = Bad EDC.

- Processing stops only on sector boundaries. The block decoding function writes data blocks of 2048 bytes to the SDRAM. The first wrong sector and all following sectors are not written to the SDRAM.
- Once FinishedFlag = 1, ErrorCode = 0 and NumSectors matches the requested number of sectors, all processed sectors can be read from the NAV Data Register. The first byte is located in the l.s. byte of the first 16-bit word in the NAV Data Register.
- This process is concluded when an **end_playback** command is issued.

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14.11 Also For: DVD Navigation File Sectors

If the bitstream is DVD navigation file sectors (*CBSelect* = 00110b), the function of the **ZR36710** becomes extracting the relevant data and providing it to the host. The following steps are done to achieve this:

- The NAV buffer is resized to be 128KBytes in this mode of operation.
- The **NAVREADY** bit of the ISR may be ignored since no NV_PCK data will be provided.
- A **start** host command begins bitstream transfer to the device.
- The **ZR36710** extracts the auxiliary data and writes it to the NAV buffer in SDRAM.
- Once a 2KByte sector has been transferred to the SDRAM, a 6-bit counter (**DVPGPFL[5:0]** in the **STATUS2** register) is incremented by 1.
- After the counter reaches 63 (i.e. 63 x 2KBytes in the NAV buffer), the counter will be set to 0 after the next sector transfer, completely filling the 128KByte buffer.
- At any time the host can read the data from the NAV buffer. To do so, the host writes to the NAV Address Register to set the base address within the NAV buffer to begin reading from and then begins reading data from the NAV Data Register as explained in Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”. The address and amount of data should be determined by the counter. For example, if the counter is 6, then the host should set the address to the beginning of the NAV buffer and read 12KBytes of data.
- An **end_playback** command ends this process.

14.12 Also For: MPEG Video Elementary Streams

If the bitstream is an MPEG video elementary stream (*CBSelect* = 01100b), the following applies:

- A/V sync is disabled since no timestamps exist within the bitstream The ADP output is muted and the video data is decoded and output as it is received.
- The **NAVREADY** bit of the ISR may be ignored since no NV_PCK data will be provided in a video elementary stream.
- The sub-picture decoder is disabled since sub-picture data does not exist in a video elementary stream.
- Only the **VCBE** and **VCBF** bits of the **STATUS0** register are relevant regarding buffer empty/full indication. **ACBE**, **ACBF, DRAMBF** and **SPCBF** are irrelevant.
- The **NAVBUF**, **HLI_TIME** and **SPDERR** bits of the **STATUS1** register are irrelevant.
- The end of the bitstream is met when the DVP parses a sequence_end_code.

14.13 Also For: Audio Elementary Streams

If the bitstream is an MPEG audio elementary stream (*CBSelect* = 01111b), an AC-3 audio elementary stream (*CBSelect* = 10110b) or a LPCM elementary stream (*CBSelect* = 11000b), the following applies:

- A/V sync is disabled since no video exists within the bitstream. The ADP begins output of the decoded data as it receives it.
- The **NAVREADY** and **DVPOBF** bits of the ISR may be ignored since no relevant video data will be provided in an elementary audio stream.
- The sub-picture decoder is disabled since sub-picture data does not exist in elementary audio streams.
- Only the **ACBE** and **ACBF** bits of the **STATUS0** register are relevant regarding buffer empty/full indication. **VCBE**, **VCBF, DRAMBF** and **SPCBF** are irrelevant.
- **C-STATE** can only have the following values: 10 1000b (***Nspb*** - no video), 01 1000 (***Pause*** - no video) during decoding.
- The **PICTYPE**, **FRAME/FIELD#**, **DVPVAL**, **NAVBUF**, **HLI_TIME** and **SPDERR** bits of the **STATUS1** register are irrelevant.
- The end of the bitstream is met only when the **end_playback** host command is issued.

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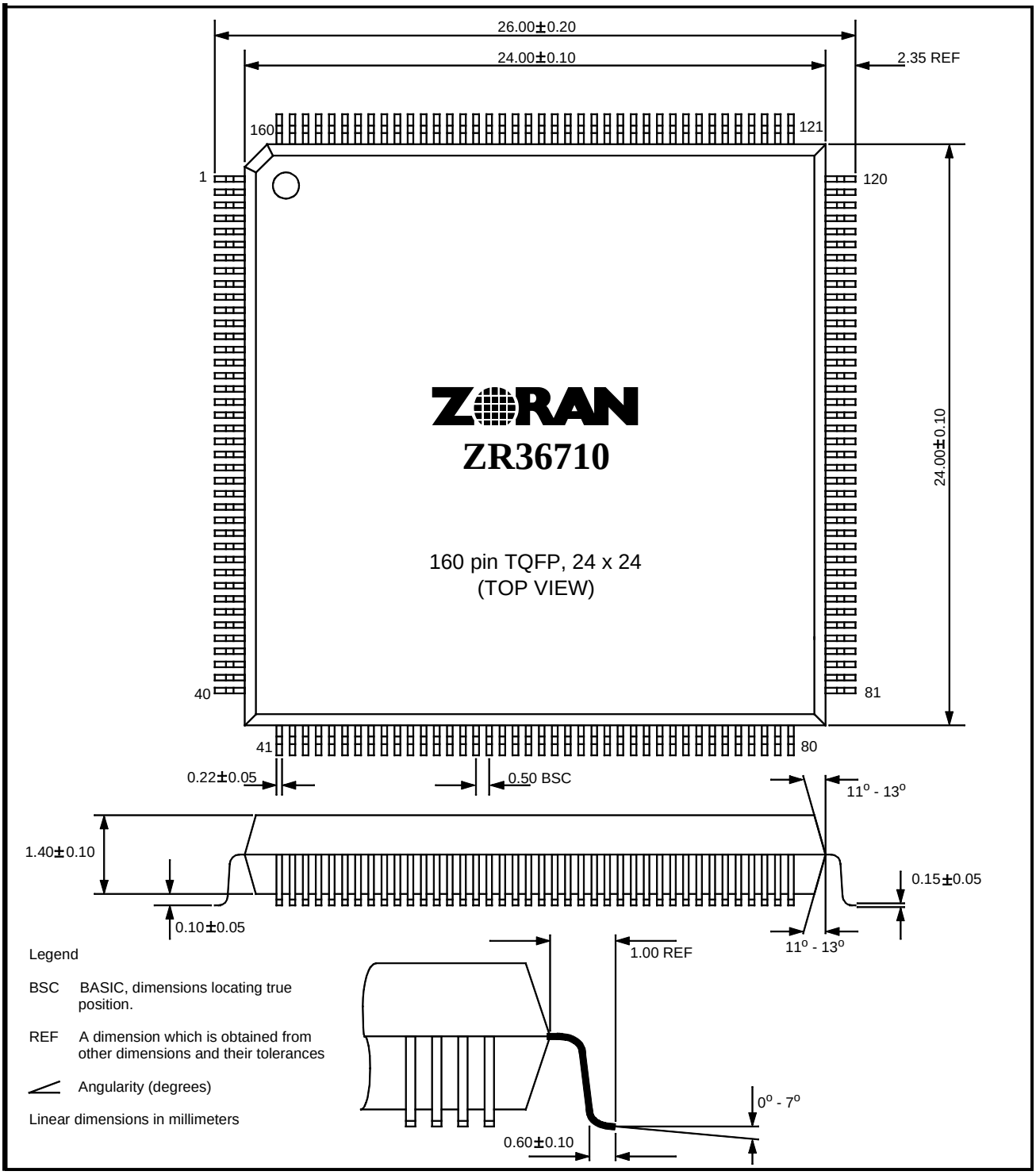
15. Annex D: Package Drawing



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